Voltage and Frequency Control of Embedded Low-Voltage Islanded Grids with Power-Electronic Generation Units
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Abstract

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This work provides a new controller design for three-phase inverter-based generation in low-voltage grids with linear and nonlinear loads below the inverter nominal power. Both voltage and frequency control loops are based on the simplification of the inner current control loop irrespective of the used inverter hardware. Despite existing design methods for voltage frequency control loops, the new design only requires the knowledge of the inverter nominal power rating and the bandwidth of the inner current control loop, whereas the latter can also be estimated. The transferability and scalability is demonstrated with an analytical and simulation based control stability analysis for inverters from 1 kW to 100 kW. In simulation and experimental tests, the new controller design is able to maintain nominal values for symmetrical resistive, resistive-inductive and resistive-capacitive loads up to the inverter nominal power and also for nonlinear constant power loads. Experimental tests with an 8 kW inverter using a standard LCL filter without transformer and an intentionally sub-optimally designed LC filter including transformer underline the transferability of the design for different hardware setups.

A novel multiple inverter control strategy for cooperative voltage and frequency control is developed which incorporates islanding operation for single and multiple inverter setups without the need for communication. The novel voltage and frequency control is based on a Master/Follower and a dead-band concept. Followers have the full potential of the Master but only use it when necessary. This concept allows to maintain nominal voltage without communication and without circulating steady-state currents among the inverter units. A procedure from zero-voltage condition is developed which allows to use the full potential of controllable power in the whole island to conjointly reach nominal grid voltage. With this, islanding operation for loads that are larger than the largest inverter but still smaller than the sum of all connected inverters is possible. In experimental tests of up to 6 kW nominal power, two inverters were able to reach nominal voltage and frequency within 200 milliseconds for a linear symmetrical load that was larger than each of the inverters. Voltage and frequency were controlled at nominal values during several load changes and even in open circuit condition. Despite existing master-slave approaches, the novel control strategy is able to compensate an outage of the Master unit. Experimental tests in the laboratory demonstrated that subsequently to a Master outage the Follower detects voltage and frequency deviations and drives them back to nominal values.

Furthermore, a new countermeasure against an excess of active power due to non-controllable inverters is presented. It can be used for all inverters in low-voltage grids that provide active reduction due to over-frequency in accordance with the grid codes. This allows to operate islanded grids that have non-controllable inverters which provide almost twice as much active power as needed by the linear resistive loads. The presented functionality is validated in simulation and in experimental tests for a 4 kW system.

Intentional islanding operation, low-voltage ride-through capability (LVRT) and anti-islanding detection (AID) have conflicting aims during grid faults. For grid integration purposes, a novel concept was proposed which provides a possible solution for those conflicting aims with the help of a time decoupling. A case study initially shows that the effectiveness of AID is not undermined if LVRT is implemented simultaneously. Subsequently to the fault behaviour, the novel islanding control strategies of this thesis can be initiated. In laboratory tests, the novel concept is demonstrated for an 8 kW inverter setup. Finally, open issues and future challenges of intentional islanding operation in low-voltage grids are provided.
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<td>A</td>
<td>current measurement unit</td>
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<td>abc</td>
<td>natural frame</td>
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<td>AID</td>
<td>anti-islanding detection</td>
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<tr>
<td>CC</td>
<td>current controller</td>
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<tr>
<td>CPL</td>
<td>constant power load</td>
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<tr>
<td>DC</td>
<td>direct current</td>
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<tr>
<td>DG</td>
<td>distributed generation</td>
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<tr>
<td>dq</td>
<td>synchronous reference frame</td>
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<tr>
<td>DS</td>
<td>dSpace</td>
</tr>
<tr>
<td>EHV</td>
<td>extra high-voltage</td>
</tr>
<tr>
<td>F</td>
<td>follower</td>
</tr>
<tr>
<td>FSPC</td>
<td>frequency shift power control</td>
</tr>
<tr>
<td>HV</td>
<td>high-voltage</td>
</tr>
<tr>
<td>IEEE</td>
<td>Institute of Electrical and Electronics Engineers</td>
</tr>
<tr>
<td>IGBT</td>
<td>insulated-gate bipolar transistor</td>
</tr>
<tr>
<td>LC</td>
<td>filter composed of a series inductor and a parallel capacitor</td>
</tr>
<tr>
<td>LCL</td>
<td>filter composed of a series inductor, parallel capacitor and series inductor</td>
</tr>
<tr>
<td>LPF</td>
<td>low-pass filter</td>
</tr>
<tr>
<td>LV</td>
<td>low-voltage</td>
</tr>
<tr>
<td>LVRT</td>
<td>low-voltage ride-through</td>
</tr>
<tr>
<td>LVRT mode</td>
<td>mode in which the inverter provides reactive current only</td>
</tr>
<tr>
<td>M</td>
<td>master</td>
</tr>
<tr>
<td>MMO</td>
<td>multiple master operation</td>
</tr>
<tr>
<td>Mosfet</td>
<td>metal-oxide-semiconductor field-effect transistor</td>
</tr>
<tr>
<td>MPPT</td>
<td>maximum power point tracking</td>
</tr>
<tr>
<td>MV</td>
<td>medium-voltage</td>
</tr>
<tr>
<td>NCG</td>
<td>non-controllable generation</td>
</tr>
<tr>
<td>NDZ</td>
<td>non-detection zone</td>
</tr>
<tr>
<td>OP</td>
<td>operating point</td>
</tr>
<tr>
<td>P(f)</td>
<td>control of active power as a function of the frequency</td>
</tr>
<tr>
<td>PCC</td>
<td>point of common coupling</td>
</tr>
<tr>
<td>PI</td>
<td>proportional integral controller</td>
</tr>
<tr>
<td>PLL</td>
<td>phase-locked loop</td>
</tr>
<tr>
<td>PR</td>
<td>proportional resonant controller</td>
</tr>
<tr>
<td>PV</td>
<td>photovoltaic</td>
</tr>
<tr>
<td>PWM</td>
<td>pulse width modulation</td>
</tr>
<tr>
<td>Q(P)</td>
<td>control of reactive power as a function of active power</td>
</tr>
<tr>
<td>Q(V)</td>
<td>control of reactive power as a function of voltage</td>
</tr>
<tr>
<td>RLC</td>
<td>resonant circuit of RLC components</td>
</tr>
<tr>
<td>RMS</td>
<td>root mean square</td>
</tr>
<tr>
<td>SMA</td>
<td>solar inverter manufacturer</td>
</tr>
<tr>
<td>SMO</td>
<td>single master operation</td>
</tr>
<tr>
<td>Acronym</td>
<td>Description</td>
</tr>
<tr>
<td>---------</td>
<td>-------------</td>
</tr>
<tr>
<td>SMS</td>
<td>slip mode frequency shift</td>
</tr>
<tr>
<td>UPS</td>
<td>uninterruptible power supply</td>
</tr>
<tr>
<td>V</td>
<td>voltage measurement unit</td>
</tr>
<tr>
<td>VC</td>
<td>voltage controller</td>
</tr>
<tr>
<td>VDE</td>
<td>Association for Electrical, Electronic &amp; Information Technologies</td>
</tr>
<tr>
<td>ZIP</td>
<td>model for constant impedance, constant current and constant power</td>
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## List of Symbols

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<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
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<td>$a_{Z,1,p}$</td>
<td>parameters of the ZIP model</td>
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<tr>
<td>$C$</td>
<td>capacitance per phase</td>
<td>F</td>
</tr>
<tr>
<td>$c$</td>
<td>design constant for time delay of Master units</td>
<td>W · s</td>
</tr>
<tr>
<td>$C_{\text{Base}}$</td>
<td>base capacitance</td>
<td>F</td>
</tr>
<tr>
<td>$C_{\text{DC}}$</td>
<td>DC-link capacitance</td>
<td>F</td>
</tr>
<tr>
<td>$C_F$</td>
<td>filter capacitance</td>
<td>F</td>
</tr>
<tr>
<td>$C_{\text{norm}}$</td>
<td>capacitance that results in resonant frequency 50 Hz</td>
<td>F</td>
</tr>
<tr>
<td>$E^*$</td>
<td>grid voltage amplitude</td>
<td>V</td>
</tr>
<tr>
<td>$e$</td>
<td>Euler’s number</td>
<td>1</td>
</tr>
<tr>
<td>$\Delta f$</td>
<td>frequency deviation</td>
<td>Hz</td>
</tr>
<tr>
<td>$f$</td>
<td>frequency</td>
<td>Hz</td>
</tr>
<tr>
<td>$f_{\text{new}}$</td>
<td>new frequency reference value</td>
<td>Hz</td>
</tr>
<tr>
<td>$F_{\text{CC}}$</td>
<td>transfer function of the current controller</td>
<td>V · A$^{-1}$</td>
</tr>
<tr>
<td>$F_{\text{CF}}$</td>
<td>transfer function of the filter capacitance</td>
<td>V · A$^{-1}$</td>
</tr>
<tr>
<td>$f_{\text{F, res}}$</td>
<td>resonant frequency of the LCL filter</td>
<td>Hz</td>
</tr>
<tr>
<td>$f_i$</td>
<td>islanding frequency</td>
<td>Hz</td>
</tr>
<tr>
<td>$F_{\text{Lg}}$</td>
<td>transfer function of the grid side filter component</td>
<td>Ω$^{-1}$</td>
</tr>
<tr>
<td>$F_{\text{Li}}$</td>
<td>transfer function of the inverter side filter component</td>
<td>Ω$^{-1}$</td>
</tr>
<tr>
<td>$f_m$</td>
<td>middle frequency of slip mode frequency shift algorithm</td>
<td>Hz</td>
</tr>
<tr>
<td>$f_{\text{max}}$</td>
<td>maximum frequency</td>
<td>Hz</td>
</tr>
<tr>
<td>$f_{\text{meas}}$</td>
<td>measured frequency</td>
<td>Hz</td>
</tr>
<tr>
<td>$f_{\text{min}}$</td>
<td>minimum frequency</td>
<td>Hz</td>
</tr>
<tr>
<td>$F_{\text{PWM}}$</td>
<td>approximated transfer function of the sample and hold and PWM unit</td>
<td>1</td>
</tr>
<tr>
<td>$f_{\text{PWM}}$</td>
<td>PWM frequency</td>
<td>Hz</td>
</tr>
<tr>
<td>$f_{\text{res}}$</td>
<td>resonant frequency of the RLC resonant circuit</td>
<td>Hz</td>
</tr>
<tr>
<td>$F_{S,V}(s)$</td>
<td>system transfer function of the voltage control loop</td>
<td>1</td>
</tr>
<tr>
<td>$F_{\text{VC}}(s)$</td>
<td>transfer function of the voltage controller</td>
<td>A · V$^{-1}$</td>
</tr>
<tr>
<td>$F_{W,V}$</td>
<td>closed loop transfer function of voltage control loop</td>
<td>1</td>
</tr>
<tr>
<td>$h$</td>
<td>PLL integrator gain</td>
<td>V$^{-1}$</td>
</tr>
<tr>
<td>$I$</td>
<td>root mean square of current</td>
<td>A</td>
</tr>
<tr>
<td>$i_{abc}$</td>
<td>phase currents in natural frame</td>
<td>A</td>
</tr>
<tr>
<td>$i^+_{abc}$</td>
<td>positive sequence current in natural frame</td>
<td>A</td>
</tr>
<tr>
<td>$i^-_{abc}$</td>
<td>negative sequence current in natural frame</td>
<td>A</td>
</tr>
<tr>
<td>$I_{\text{Base}}$</td>
<td>base current</td>
<td>A</td>
</tr>
<tr>
<td>$i_d$</td>
<td>direct component of the current, active current</td>
<td>A</td>
</tr>
<tr>
<td>$i_d(t)$</td>
<td>time varying direct component of the current</td>
<td>A</td>
</tr>
<tr>
<td>$i^*_{dq}$</td>
<td>current reference value in dq axes</td>
<td>A</td>
</tr>
</tbody>
</table>
\( i_{dq}^+ \) positive sequence current in synchronous reference frame A
\( i_{dq}^- \) negative sequence current in synchronous reference frame A
\( i_{dq}^* \) positive sequence reference current in synchronous reference frame A
\( i_{dq}^- \) negative sequence reference current in synchronous reference frame A

\( L_g \) complex grid side current A
\( i_{LVRT}^* \) additional reactive current during an LVRT A
\( i_q \) quadrature component of the current, reactive current A
\( i_q(t) \) time varying quadrature component of the current A
\( i_q^\sim \) reactive current of the load A
\( i_{q,0}^* \) reactive current before an LVRT A
\( i_{q,C} \) reactive current for capacitance A
\( i_{q,ind} \) reactive current for inductance A
\( i_{q,max} \) maximum reactive current of the inverter A
\( k \) k-factor for the calculation of LVRT reactive current 1

\( K_{50,2} \) proportional gain of the frequency reference controller Hz \( \cdot \) V\(^{-1} \)
\( k_d \) droop control coefficients direct axis W \( \cdot \) s
\( K_I \) integral gain of the current controller V \( \cdot \) A\(^{-1} \) \( \cdot \) s\(^{-1} \)
\( K_{I,V} \) integral gain of the voltage controller A
\( K_P \) proportional gain of the current controller V \( \cdot \) A\(^{-1} \)
\( K_{P,V} \) proportional gain of the voltage controller A \( \cdot \) V\(^{-1} \)
\( k_q \) droop control coefficients quadrature axis var \( \cdot \) s
\( K_S \) system gain A \( \cdot \) V\(^{-1} \)
\( K_{S,f} \) plant gain for frequency changes s\(^{-1} \) A\(^{-1} \)
\( K_{S,f,cap} \) capacitive plant gain for frequency changes F\(^{-1} \) V
\( K_{S,f,ind} \) inductive plant gain for frequency changes s\(^{-2} \) H V\(^{-1} \)
\( K_{S,V} \) system gain for voltage control loop Ω
\( L \) inductance per phase H
\( l_{cable} \) cable length m
\( L_F \) sum of filter inductances of an LCL filter H
\( L_g \) grid side inductance H
\( L_i \) inverter side inductance H
\( m_{abc} \) modulation signal in natural frame 1
\( m_{dq} \) modulation signal in synchronous reference frame 1
\( m_{dq}^+ \) positive sequence modulation signals in synchronous reference frame 1
\( m_{dq}^- \) negative sequence modulation signals in synchronous reference frame 1

\( \Delta P \) active power provided from the grid W
\( P \) active power W
\( P^* \) active power reference value W
\( p \) design parameter of the lead compensators rad
\( P_0 \) actual operation point active power W
\( P_0^\prime \) active power before a frequency change W
\( P_{act} \) actual active power W
\( P_F \) active power of the Followers W
\( P_G \) active power of the generators W
\( P_I \) active power of the I component W
$P_{\text{inv}}$ active power of the inverter W

$P_{\text{inv}}(t)$ time varying active power of the inverter W

$P_L$ active power demand of the load W

$P_L(t)$ time varying active power demand of the load W

$P_M$ active power of the Master W

$\Delta P_{\text{max}}$ maximum active power provided from the grid W

$P_{\text{max}}$ maximum active power of the inverter W

$P_n$ nominal power W

$P_{\text{NCG}}$ active power of the non-controllable generation W

$P_{\text{NCG},0}$ active power of the non-controllable generation before a frequency change W

$P_{\text{NCG},\text{max}}$ maximum active power of the non-controllable generation W

$P_{\text{NCG},\text{max,ext}}$ extended maximum active power of the non-controllable generation W

$P_{\text{NCG, min}}$ minimum active power of the non-controllable generation W

$P_{\text{NCG}, n}$ nominal power of the non-controllable generation W

$P_P$ active power of the P component W

$P_{\text{ref}}$ reference value of the active power W

$P_Z$ active power of the Z component W

$\Delta Q$ reactive power provided from the grid var

$Q$ reactive power var

$Q^*$ reactive power reference value var

$Q_0$ actual operation point reactive power var

$Q_C$ capacitive reactive power var

$Q_f$ quality factor of the $RLC$ resonant circuit 1

$Q_G$ reactive power of the generators var

$Q_{\text{ind}}$ inductive reactive power var

$Q_{\text{inv}}$ reactive power of the inverter var

$Q_{\text{inv}}(t)$ time varying reactive power of the inverter var

$Q_L$ reactive power demand of the load var

$Q_L(t)$ time varying reactive power demand of the load var

$Q_{\text{max}}$ maximum reactive power of the inverter var

$Q_{\text{RLC}}$ reactive power of the load var

$R$ resistance per phase Ω

$R'$ resistance per length Ω·km$^{-1}$

$R_{\text{ch}}$ chopper resistance Ω

$R_F$ sum of filter resistances of an $LCL$ filter Ω

$R_L$ load resistances Ω

$R_{\text{ff}}$ virtual resistor (used for virtual admittance) Ω

$R_g$ grid side filter resistance Ω

$R_i$ inverter side filter resistance Ω

$r_T$ transformer ratio 1

$s$ laplace operator s$^{-1}$

$S_{\text{max}}$ maximum apparent power V·A

$t$ time s

$t_{0,1,2}$ starting time of an event s

$T_1$ time constant of the filter components s

$t_{\text{delay}}$ time delay before Followers join the Master s

$t_{f,\text{stable}}$ time when integral term of Follower frequency controller is deactivated s
flexible time delay dependent on inverter size

time after Master and Followers shut down if voltage is not OK

maximum restoration time of frequency control loop

current PI controller time constant

voltage PI controller time constant

random time offset for delay of Master units

recovery time before an inverter starts injecting power

sampling time

safety margin time delay

agreed service voltage

voltage

peak voltage

root mean square of grid voltage

voltage reference value

voltage

DC-link voltage

minimum DC-link voltage

reference value of the DC-link voltage

positive sequence voltage in natural frame

negative sequence voltage in natural frame

base voltage

filter capacitance voltage

complex filter capacitance voltage

direct component of the voltage in synchronous reference frame

time varying direct component of the voltage

nominal active voltage component

DC-link voltage

minimum DC-link voltage

reference value of the DC-link voltage

positive sequence voltage in synchronous reference frame

negative sequence voltage in synchronous reference frame

grid voltage

time dependent root-mean-square grid voltage line-to-neutral

islanding voltage

voltage before LVRT event

voltage limit that activates frequency raise

time dependent minimum required LVRT voltage

upper limit of voltage range

lower limit of voltage range

line-to-line root-mean-square voltage

quadrature component of the voltage in synchronous reference frame

time varying quadrature component of the voltage

maximum reactive voltage component of the PLL

complex terminal voltage

reactance

reactance per length

complex parallel reactance

reactance inductive or capacitive
<table>
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<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>$X_{C,RL}$</td>
<td>complex reactance of capacitor or resistor and inductance</td>
<td>Ω</td>
</tr>
<tr>
<td>$X_{ff}$</td>
<td>virtual reactance (used for virtual admittance)</td>
<td>Ω</td>
</tr>
<tr>
<td>$X_{L,ges}$</td>
<td>nominated inductive impedance of the LCL filter</td>
<td>Ω</td>
</tr>
<tr>
<td>$Z$</td>
<td>impedance</td>
<td>Ω</td>
</tr>
<tr>
<td>$Z_{Base}$</td>
<td>base impedance</td>
<td>Ω</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>design parameter of the lead compensators</td>
<td>1</td>
</tr>
<tr>
<td>$\delta$</td>
<td>derivative operator</td>
<td>-</td>
</tr>
<tr>
<td>$\delta_m$</td>
<td>phase shift of the lead compensators</td>
<td>°</td>
</tr>
<tr>
<td>$\omega$</td>
<td>angular frequency</td>
<td>rad</td>
</tr>
<tr>
<td>$\omega^*$</td>
<td>angular frequency reference value</td>
<td>rad</td>
</tr>
<tr>
<td>$\omega^+$</td>
<td>positive sequence angular frequency</td>
<td>rad</td>
</tr>
<tr>
<td>$\omega^-$</td>
<td>negative sequence angular frequency</td>
<td>rad</td>
</tr>
<tr>
<td>$\omega_0$</td>
<td>actual operation point angular frequency</td>
<td>rad</td>
</tr>
<tr>
<td>$\omega_c$</td>
<td>cutoff frequency of the PLL (bandwidth)</td>
<td>rad</td>
</tr>
<tr>
<td>$\omega_n$</td>
<td>nominal angular frequency</td>
<td>rad</td>
</tr>
<tr>
<td>$\tau'$</td>
<td>system time constant of the voltage control loop</td>
<td>s</td>
</tr>
<tr>
<td>$\tau_{50.2}$</td>
<td>time constant of the frequency reference control</td>
<td>s</td>
</tr>
<tr>
<td>$\tau_l$</td>
<td>time constant of frequency restoration control loop</td>
<td>s</td>
</tr>
<tr>
<td>$\tau_i$</td>
<td>time constant of the current control loop</td>
<td>s</td>
</tr>
<tr>
<td>$\tau_{i,guess}$</td>
<td>estimated time constant of the current controller</td>
<td>s</td>
</tr>
<tr>
<td>$\tau_{PWM}$</td>
<td>approximated time constant of the sample and hold and PWM</td>
<td>s</td>
</tr>
<tr>
<td>$\tau_V$</td>
<td>time constant of the voltage control loop</td>
<td>s</td>
</tr>
<tr>
<td>$\varphi$</td>
<td>phase angle</td>
<td>rad</td>
</tr>
<tr>
<td>$\varphi_{Load}$</td>
<td>phase angle of the RLC resonant load</td>
<td>°</td>
</tr>
<tr>
<td>$\varphi_{max}$</td>
<td>maximum phase angle of slip mode frequency shift algorithm</td>
<td>°</td>
</tr>
<tr>
<td>$\varphi_{SMS}$</td>
<td>actual phase angle of slip mode frequency shift algorithm</td>
<td>°</td>
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</tbody>
</table>
Chapter 1

Introduction

The amount of distributed generation (DG) is constantly increasing. In some countries, such as Germany, incentives have been introduced in order to encourage the installation of small, distributed power plants. Figure 1.1 shows the amount of installed power of generation units that benefit from financial incentives in accordance with the renewable energy law in Germany [1]. By the end of the year 2015, more than 92 GW of renewable energy plants have been connected to German grids. Almost half of the power is connected to medium-voltage grids. But low-voltage generation units have a significant share, too. There are more than 1.5 million photovoltaic (PV) power plants connected to low-voltage grids. This represents almost 96% of all generators in Germany. As shown in Figure 1.2, small and medium size inverters with a nominal power of less than 20 kW comprise most of the DG—more than 1.2 million units.

The increase in DG—especially in low-voltage grids—leads to big challenges for the design, expansion and operation of energy supply. Integrating DG into the grid will be of high importance within the next decades. But despite the challenges, DG offers a lot of potential that can be used. Smaller generators are increasingly responsible for ancillary services such as active power reduction in case of over-frequency and the allocation of reactive power. In addition, low-voltage ride-through (LVRT) capability is becoming increasingly relevant—even in low-voltage grids.

In some parts of the grid, power generation is even higher than the power demand. This leads to temporary reverse energy flow towards higher voltage levels. Normally, this causes inconveniences for distribution grids, as this can lead to the violation of voltage limits. But

![Figure 1.1: Installed power of generation units for grid layers in Germany. Numbers in accordance with the German renewable energy law. LV: low-voltage, MV: medium voltage, HV: high-voltage, EHV: extra high-voltage.](image-url)
reverse energy flows also imply, that this part of the grid has the potential to provide itself with a sufficient amount of energy.

In the past, a surplus of power coming from DG evoked new problems because a potential balance of power can lead to unintentional islanding when small parts of the grid are disconnected from the rest of the utility grid. Prior to the growth of DG, islanded grids collapsed because no generation was available. But recently DG is getting the potential to temporarily cover the load demand. However, the accidental operation of islanded grids has not been desired yet and thus protection devices and algorithms have been developed to avoid this. This was called anti-islanding detection (AID).

Unlike unintentional islanding, intentional islanding has been long-established. Uninterruptible power supplies provide electricity to local customers during grid outages. This concept has also been introduced on a larger scale. So-called microgrids try to provide additional technical and economical benefits for their customers by intentional standalone operation, independent of the grid. Thus, intentional islanding operation offers benefits—especially when used as a backup system.

1.1 Problem Statement and Objectives of this Work

The big majority of customers in low-voltage grids does not benefit from the advantages of intentional islanding operation. There is a large amount of DG in low-voltage grids but those generators usually are not designed for islanding operation. Most of it is inverter-based generation such as in PV plants. Thus, a lot of potential generation cannot be used for islanding purposes because the implemented inverter control does not incorporate the required voltage and frequency control which is crucial for the operation of islands. Thus, if it is desired to provide intentional islanding operation in low-voltage grids, it might be necessary to equip the existing inverters with voltage and frequency control loops to maintain operation at nominal values 230/400 V, 50 Hz. But there are some problems to overcome:

- Low-voltage grid structures are diverse and the loads in these grids show diverse behaviour. There are loads that show linear resistive, inductive or capacitive behaviour. Furthermore, the share of switch-mode power supplies—so-called constant power loads (CPL)—is relatively high. Asymmetrical load conditions are a big problem. In addition, there might
be motor drives that vary significantly from other load types, especially during start-up phase.

- The characteristics of low-voltage inverters are also diverse. Old stock inverters might have different hardware setups such as filter topologies (L, LC or LCL filter) and transformers. There might be complex current control strategies incorporating multiple current measurement points (e.g. grid- and inverter-side current) or active harmonic damping. In summary, the manifold improvements of inverter operation resulted in various topologies. This means that for an optimum islanding operation design, every product would require a separate design for the voltage and frequency control loop.

- The number of inverters in low-voltage grids is relatively high and there could be multiple inverters in the same island. Thus, it could be challenging to combine several specialised controls into a conjoint control and prevent undesired interferences.

Due to the mentioned reasons, it might be more promising to reconcile the inverters with the help of a unified voltage and frequency controller design. This could be used not only for a single product but for various inverters. Thereby a supervisory control strategy for multiple inverter operation could be designed. Besides, a conjoint control approach could be of advantage if the outage of a single inverter needs to be balanced by other inverters.

Hence, the objective of this thesis is to provide a novel voltage and frequency control loop of low-voltage islanding operation with inverter-based generation units. The novel control strategy is supposed to provide robust and stable islanding operation in accordance with control theory for different linear and nonlinear load conditions if the primary power supply is higher than the power demand. It is intended to provide a design approach that can be used for several inverter filter and transformer hardware setups and current controller designs. The control strategy aims for incorporating a concept for conjoint voltage and frequency control for multiple inverter operation. Another objective is to provide a new concept for the simultaneous implementation of low-voltage ride-through (LVRT) capability, effective detection of unintentional islanding (AID) and subsequent intentional islanding operation.

1.2 Approach and Methodology

Figure 1.3 illustrates the methodology of voltage and frequency control loop design for low-voltage islanding operation. Initially, a modelling process is executed to derive models for the three main topics of the development process: single inverter operation, multi inverter operation and grid integration. These three topics are elaborated in the following blocks (grey boxes).

Based on a literature search, state-of-the-art inverter control is compared to requirements and limitations for a single inverter operation. Due to limitations of existing design methods, a new design concept is developed. Validation of the single inverter control focuses on its transferability and scalability, i.e. that the proposed design process can be used for different current control loops, filter and/or transformer setups and inverter nominal powers.

For multiple inverter operation, additional requirements and initial conditions are compiled. A novel voltage and frequency control strategy including a procedure from zero-voltage condition is developed. The validation process is used to evaluate several key capabilities that are important for islanding operation incorporating both single and multiple inverter operation.

Finally, a novel integration concept for the conjoint implementation of existing grid codes (anti-islanding detection, AID), future grid codes (low-voltage ride-through, LVRT) and intentional
islanding operation incorporating the novel control is proposed. The validation focuses on the compatibility of the novel islanding control strategy and the requirements of grid support. Finally, open issues and future challenges are derived.
1.3 Contributions and Limitations

In this thesis, the following contributions are provided:

1. A new controller design for voltage and frequency control loop of inverter-based generation (Validation: simulation and analytical for up to 100 kW, experimental for up to 8 kW nominal power),

2. Transferability and scalability of the design for different inverter hardware setups and power ratings (Validation: simulation and analytical for up to 100 kW, experimental for up to 8 kW nominal power),

3. A novel multiple inverter control strategy for cooperative voltage and frequency control without communication (Validation: simulation and experimental for up to 6 kW nominal power),

4. A new countermeasure against an excess of active power due to non-controllable generation (Validation: simulation, analytical, experimental for up to 4 kW nominal power),

5. A novel concept for the grid integration concept of simultaneous implementation of low-voltage ride-through, anti-islanding detection and islanding operation (Validation: simulation, analytical, experimental for up to 8 kW nominal power)

The contributions can be classified into three groups: single inverter operation (contribution 1 and 2), multiple inverter operation (contribution 3 and 4) and grid integration (contribution 5).

Single Inverter Operation (1, 2)

There are various design methods for voltage and frequency control in islanding operation. Existing methods use an extensive design incorporating the inverter’s hard- and software including filter design and the current control loop. Even so-called unified design methods are of high complexity and/or are designed for a specific critical load incorporating extra load current measurements. The benefit of these elaborated approaches is that the whole control loops are optimised for the actual islanding conditions and thus provide a high level of controllability and voltage and frequency quality.

In this thesis, a new controller design for the voltage and frequency control loop of inverter-based generation is presented. Adding the proposed voltage and frequency control loop allows to transform grid feeding units into grid forming units. The designed grid forming units are able to operate under islanded conditions for resistive, resistive-inductive and resistive-capacitive loads as long as the load does not exceed the nominal power rating of the inverter. Furthermore, islanding operation is also demonstrated for nonlinear constant power loads. Despite existing design methods for voltage and frequency control loops, the proposed controller design only requires a minimum knowledge of the underlying inverter. The design process is independent of the actual filter and current control loop design. No current measurement or hardware changes of the filter are required. For the design process, only the nominal power of the inverter and the current control time constant are required, whereas the latter can also be estimated.

Both voltage and frequency control loops use virtual feed-forward admittances which make the control stable for the relevant load conditions. The new controller design is based on the assumption that the behaviour of the current control loop can be estimated by a first order lag element with a specific time constant $\tau_i$. It is shown that even if this time constant is unknown
and needs to be estimated, the voltage control loop remains stable according to standard control theory. Thus, the new design method provides a high level of control robustness.

The transferability and scalability of the proposed controller design is demonstrated. Standard LCL filter design rules are used to estimate filter setups for 1 kW, 10 kW and 100 kW inverters. The new voltage and frequency control loops are tested for these nominal powers by the analysis of the transfer function of each inverter size and by simulations. Besides, the new controller design was experimentally tested for a sub-optimal LC filter and transformer design to show its transferability to other hardware setups.

Experimental tests in the laboratory are executed for linear symmetrical RLC loads and non-linear three-phase constant power loads up to 8 kW. The experiments show that nominal voltage and frequency is reached within 100 ms and 200 ms respectively. Symmetrical load steps of both linear and nonlinear loads can be managed by the proposed controllers and voltage and frequency are controlled to nominal values.

Multiple Inverter Operation (3, 4)

Popular methods for the operation of multiple inverters in parallel are the droop control method and the master-slave approach. The droop control incorporates hierarchical control which requires communication and thus fails to maintain nominal values if there is no communication link to the secondary controller. The master-slave approach usually is not able to compensate for an outage of the master if there is no communication between the master and slave units. Hence, both methods might not be the best choice for a control strategy which is not based on communication.

A novel multiple inverter control strategy for cooperative voltage and frequency control is developed which incorporates islanding operation for single and multiple inverter setups. A procedure from zero-voltage condition is proposed which allows to determine which of the inverters is supposed to become the Master unit and initiates islanding. The other units become so-called Followers but keep full capability of the Master. Both the cooperative voltage and frequency control and the procedure from zero-voltage do not need communication.

The procedure from zero-voltage condition combines the active power of all inverters that are equipped with the novel control. This allows to start islanding operation for loads that are larger than the largest inverter but still smaller than the sum of all connected inverters. This distinguishes the proposed method from existing master-slave approaches, in which the master unit has to provide the full power unsupported.

The cooperative voltage control is based on a dead-band concept. Inside the dead-band the Master controls voltage and frequency to nominal values with the incorporated proportional integral controller. The Followers only operate with a proportional controller. This concept allows to maintain nominal voltage without communication and without circulating steady-state currents among the inverter units. An analogue concept is used for the frequency control. As soon as the dead-band is violated, the Followers support the Master to re-establish nominal values for both voltage and frequency by activating their integral controller term. When nominal values are eventually reached, the Followers deactivate their integral controller term.

The proposed method is able to incorporate benefits of the established methods whilst avoiding some of the drawbacks. The droop control approach is able to operate without communication. But it has the disadvantage of steady-state errors which needs to be reset by a power reallocation that requires communication. The novel voltage and frequency control in this thesis does not
require a communication link but is able to maintain nominal values throughout the operation. The master-slave approach is able to operate without steady-state error, but if the master has an outage, the island collapses. In contrast to existing master-slave approaches, the proposed control strategy is able to compensate an outage of the master unit. In this case, another controllable inverter takes the lead. It detects voltage and frequency deviations and drives them back to zero.

Non-controllable generation (NCG) in an island is a possible disturbance and can result in over-voltage. An inverter manufacturer developed a countermeasure against an excess of active power which is presented in subsection 4.4.2. A master inverter imposes a frequency change in the island to indirectly communicate with other inverters which consequently reduce their active power. But the existing method for the reduction of NCG is limited to inverters of a single manufacturer and it requires the existence of a battery storage system to determine whether there is an excess of active power in an island.

In this thesis, a new control strategy for an effective countermeasure against an excess of active power has been developed. It also uses frequency changes to indirectly communicate with NCG, but the method that is introduced in this thesis uses a standardised curve which is stipulated by grid codes. Thus, every generation unit which is in accordance with the grid codes should be able to interpret the increasing frequency and reduce its active power. Besides, no battery storage system is required for the viability of the new method because the excess of active power is measured with the islanding voltage.

Experimental tests in the laboratory demonstrate that the procedure from zero-voltage condition and the conjoint voltage and frequency control are feasible in several setups of up to 6 kW nominal power. The zero-voltage procedure is able to reach nominal voltage and frequency within 150 ms in an island with one Master and one Follower inverter and a symmetrical load. Outages of the Master unit are compensated by a Follower and NCG is successfully controlled with an increase in islanding frequency.

Grid Integration and Compatibility (5)

According to actual grid codes, inverter-based generation in low-voltage grids must trip in the event of a grid fault and thus does not need to provide low-voltage ride-through capability (LVRT). However, recently new recommendations for LVRT capability of generators in low-voltage grids have been proposed. In addition, there are suggestions for separate window periods for grid faults and anti-islanding detection (AID). But whether the provision of reactive current during LVRT might cause AID to become ineffective has not been discussed yet.

A novel concept is developed in this thesis which provides a possible solution for the grid integration in combination with LVRT and AID. Recent recommendations for future LVRT behaviour are included. Conflicting aims of the three domains are dissolved and their compatibility is scrutinised with the help of a case study. In this case study, possible outcomes of both grid faults and unintentional islanding are derived. Asymmetrical faults are included and a standard active AID algorithm is used.

The conjoint implementation of LVRT, AID and intentional islanding operation is achieved by a time decoupling. It is initially shown that LVRT even improves the effectiveness of AID. In the event of a fault, the inverters provide reactive current in order to support the grid until the fault is cleared. After the fault is cleared, the inverters return to normal operation. If the fault is not cleared eventually or if the voltage and frequency behaviour signify unintentional islanding,
the inverters trip. In case the fault is actually unintentional islanding, the provision of LVRT supports its detection and leads to a fast tripping. When the low-voltage grid is disconnected from the rest of the utility grid and thus there is a zero-voltage condition, it is possible to initiate the multiple inverter procedure. Finally, intentional islanding operation is established.

In simulation, the DC-link of the inverter is modelled using a single-diode model for a PV generator. Hence, effects on the DC-link voltage due to quick changes of active and reactive power injection on the AC side are analysed. For experimental tests in the laboratory, a constant voltage source is used. Both simulation and experimental tests for up to 8 kW support the theoretical analysis of the case study and feasibility of subsequent intentional islanding operation is shown.

1.4 Structure of this Thesis

The theoretical background of this work is provided in chapter 2. Analyses on low-voltage grid structures is provided and a simplified model is derived. The voltage and frequency behaviour of islanded grids is crucial for a suitable control design, thus the mathematical and physical foundations are laid. This includes both linear and nonlinear constant power loads. Next, a categorisation of different inverter control strategies is presented. The basic control concept and differences between several system control approaches are explained. Popular methods like the droop-control concept and the master-slave concept are assessed and their drawbacks and limitations are emphasised. The theoretical background is rounded up with requirements with regard to low-voltage ride-through capability and anti-islanding detection methods.

Chapters 3, 4 and 5 contain the novelty of this thesis. In chapter 3, the new controller design for inverter-based generation is presented. A new control structure is compared to the state-of-the-art and its benefits are emphasised. The scalability, stability and robustness of the new control are demonstrated and validated with analytical models and simulations. Finally, experimental tests in the laboratory are executed.

Chapter 4 presents the novel control strategy for multiple inverter control in combination with a procedure from zero-voltage condition. Voltage and frequency control are implemented co-operatively without communication. Non-controllable generation is integrated into the control strategy and a new countermeasure against an excess of active power is presented. Tests in the laboratory confirm the findings.

In chapter 5, a novel grid integration concept is proposed. First, conflicting aims of islanding operation and grid compatibility are scrutinised. A solution for the simultaneous implementation of low-voltage ride-through, anti-islanding detection and subsequent intentional islanding operation is presented. Experimental results validate analytical deliberations. Open issues and future challenges with regard to intentional islanding operation in low-voltage grids are provided.

Finally, in chapter 6 a short conclusion of this thesis is provided.
Chapter 2

State of the Art

2.1 Isolated Power Systems in General

The transition from integrated power systems to isolated power systems is smooth because the larger isolated power systems are, the more similar they are to integrated power systems. Technically speaking, in isolated grids, the only task of the secondary controller is to restore system frequency to nominal value. In integrated power systems, an additional task of the secondary control loop is to control power flows between grid segments via interconnection lines.

Examples for isolated grids are geographical islands or remote settlements. In some literature, even on-board power systems on ships or aircrafts are included in the discussion on control approaches in isolated grids.

Geographical islands suffer from the fact that inverter-based generation replaces synchronous generation such as hydro power plants. This effect is even more important than in integrated power systems because of the relatively high fluctuations and imbalances in power generation and demand and the fact that there are no neighboring grid segments that could support during dynamics. The maximum in non-synchronous generation has a major influence on the dynamics and thus on the control approach of the power system [2]. In [3], an overview on advanced control approaches for isolated power systems is provided. Basically, the required backup power is relatively high in order to overcome the fluctuations in power demand. Whereas in the past, this was mainly implemented by over-sizing power plants, recently energy storage systems are within the focus [4, 5]. Over-sizing of power plants is a good method to increase reliability as long as the increased need for volume and weight has limited negative effects—which is the case in mobile applications. Furthermore, economic and environmental issues have an increasing influence in isolated power system design and control, leading to the necessity of an increased integration of inverter-based generation [2] or makes load shedding an interesting option [6–8]. The usage of load shedding requires controllable loads which is not always possible. Furthermore, it might become costly when a large number of loads need to be equipped with for example frequency tripping relays.

With the rise of the so-called more electric aircraft, control topologies in aircrafts have become more and more complex [9, 10]. An increasing use of power electronics results in mixed power systems that require reliable control hierarchies and strategies. Electric motor drives control is in the focus. A good overview of both technologies and control can be found in [11] and [12]. Similar to the advances on aircrafts, the idea of all-electric ships rises new challenges in the control and stability of power systems on ships [13], also using static compensators [14] or DC grids [15]. On-board power systems usually have in common, that the maximum power demand and the load characteristics are well-known and thus the generation units and the generator control can be optimised to the desired use-cases.
Recently, microgrids are more and more in the focus of control approaches. The state of the art in inverter-based microgrid control will be discussed in detail in section 2.4.

2.2 Low-Voltage Grid Structures

There has been substantial research on the propositions and the composition of low-voltage grids [16–19]. Due to the high number and possible configurations, it is quite challenging to find a suitable methodology to representatively model the behaviour of low-voltage grids. They have in common that there is a connection to the medium voltage grid—usually 10 kV in urban areas and 20 kV in rural areas.

Generally, low-voltage grid structures can be split into three main classes which are shown in Figure 2.1: string (a), ring (b) and meshed (c). Each segment consists of loads and can contain distributed generation, mainly connected via power electronics. Normally, the geometrical structure of the grid resembles the street infrastructure. In rural areas, string grid structures are most common. With increasing numbers of consumers, strings can be connected to rings. Rings are usually operated with open ends in the middle of the ring. Multiple rings with multiple feeders can be transformed into meshed grids which cause an increased effort for operation but provide additional security of supply [17,18].

In [18], representative grid structures for rural, suburban and urban grids have been investigated and developed. Examinations showed that the cable or line length from the busbar to the farthest household generally is within 150 m and 500 m. Thus, if islanding is initiated from the end of one string and a load is connected at the end of another string, the total distance between these two components is usually less than 1 km.

Reference [17] provides statistics about the used cables and lines in rural, suburban and urban grids. Cables and/or lines with cross-sections of at least 70 mm$^2$ are used with a resistance of about 0.5 $\Omega$ km and an inductance of about 0.08 $\Omega$ km. Most often, NAYY cables with cross sections of 150 mm$^2$ or more are used [20, 21]. Thus, the grids are dominated by ohmic behaviour ($3 \leq R/X \leq 7$) and the total resistance for 1 km cable or line should be below 0.5 $\Omega$.

Figure 2.1: Several grid structures for low-voltage grids. a) string, b) ring, c) meshed. Protection devices are not included here. Sub-branches are neglected [17].
In summary, the line resistance is small compared to the base impedances of loads which is 16 Ω for a 10 kW inverter. In [22], different cable types with a length up to 2 km have been simulated. It was shown that there are only minor effects on control stability and thus they have been neglected in further investigations.

Figure 2.2 shows a condensed model of low-voltage grid topologies. It is a simplification which is derived from the investigations in [16–19]. This model is used to discuss and develop the islanding operation strategy that is proposed in this thesis for single and multiple inverter operation and for a possible grid integration concept.

Irrespective of the actual islanding operation concept, splitting of the utility grid and the island is crucial. It is mandatory to provide a possibility to disconnect the low-voltage grid from the rest of the utility grid. To date, there are almost no grid structures that provide a disconnection device as illustrated in Figure 2.2. Thus, in order to transform low-voltage grids into standalone islands in the future, further research is needed to realise an optimal design of a future disconnection device. This could for example be a load switch or a circuit breaker which disconnects the grid subsequently to a fault and previously to the islanding operation. In the following investigations, it is assumed that such a disconnection device is available and that it disconnects the utility grid right before islanding operation is initiated.
2.3 Voltage and Frequency Behaviour in Islanded Grids

Due to the high level of variation in low-voltage grids, a model needs to be found that sufficiently describes the behaviour of islanded low-voltage grids. On the one hand, a wide range of possible compositions must be covered. On the other hand, the model needs to be simple in order to be able to develop and design a suitable control approach. This is achieved by using a suitable sample space.

Islanded grids consist of three major blocks:

- generation units: in this thesis only power-electronic generation units (inverters) are considered
- load units: the size and type of load can vary strongly
- interconnection: cable or line type that interconnects generation and/or load units.

Interconnections are especially of importance when designing large area microgrids with a large number of interacting generation units. In this case, line resistances and impedances influence steady state operation and in particular power sharing between generation units. Thus, there has been intensive research on this issue. For low-voltage islanding operation as investigated in this thesis, interconnections play a minor role. One reason is that the geographical size of low-voltage grids is small in comparison to microgrids that can expand up to the high-voltage level. Second, low-voltage grids have a very high $R/X$ ratio. This means, that the line/cable behaviour is mainly resistive and not inductive. This has some advantages when it comes to dynamic stability in multiple generation operation but causes some disadvantages with respect to the decoupling of active and reactive power. But the design and validation process that is used in chapter 3 is based on a large signal analysis and not on a small signal analysis. Thus, for this thesis, the electrical behaviour of the interconnections can be included into the load design.

Loads in low-voltage grids define the active and reactive power consumption of an islanded grid. There might be resistive, inductive and/or capacitive behaviour. Moreover, not only linear loads like $RLC$ components but also nonlinear loads might be part of the island. In low-voltage grids the share of switch-mode power supply is increasing [23, 24]. A big part of those loads shows so-called constant power behaviour. Hence, this type of load needs to be considered. In summary, linear and nonlinear loads define the sample space in which the proposed inverter control needs to be tested.

Generation units are in the focus of this work because the key to stable and robust islanding operation is a suitable controller design in inverter-based generation units. Furthermore, in real low-voltage islanded grids there will be existing generation units, for example older photovoltaic generation. These generators are a very important part of the island, because they strongly influence the stability and voltage and frequency behaviour of an island.

In the following, islanding behaviour will be investigated with respect to different load compositions. The results of the analysis will be used to define a representative model which can be used to validate the suitability of the proposed control strategy. Islanding operation requires stability and robustness throughout certain events that might occur before or subsequent to islanding.

Furthermore, the design of the control loops in later chapters is executed in synchronous reference frame. Hence, the voltage and frequency behaviour is also analysed with variables in the synchronous reference frame. Of course, controller design might be implemented in stationary reference frame as well but here, the synchronous reference frame allows to calculate with DC variables and supports an easier understanding.
2.3.1 Islanded Grids with Linear Loads

Figure 2.3 shows a single phase equivalent circuit of a symmetrical three phase low-voltage system with a power electronic generation unit and a linear \( RLC \) load. This model will be used to further approximate voltage and frequency behaviour in islanded grids with linear loads.

The system of Figure 2.3 obeys a strict balance of generated and consumed active and reactive power according to active power \( P_{\text{inv}} \) and reactive power \( Q_{\text{inv}} \) of the inverter and \( P_L \) and \( Q_L \) of the load.

\[
P_{\text{inv}} + Q_{\text{inv}} = P_L + Q_L + \Delta P + \Delta Q
\]  

(2.1)

In case the system is islanded by opening the main switch, neither active nor reactive power will be exchanged with the grid, \( \Delta P = \Delta Q = 0 \).

As \( P \) and \( Q \) are orthogonal components in steady state, the power balance in an islanded grid can be split into two independent parts for active and reactive power. Assuming that the loads can be described with linear electrical components such as a parallel \( RLC \)-circuit with resistive part \( R \) per phase and reactive parts \( L \) and \( C \) per phase, \( P_L \) and \( Q_L \) can be replaced:

\[
P_L = \frac{V^2}{R} \tag{2.2}
\]

\[
Q_L = V^2 \cdot \left( \frac{1}{2\pi f \cdot L} - 2\pi f \cdot C \right) \tag{2.3}
\]

where \( V \) is the root-mean-square value of the applied grid voltage and \( f \) the islanding frequency. Equation (2.2) shows that the amount of active power provided in an islanded system that only consists of power-electronic generation units and linear loads depends only on the voltage. Furthermore, (2.3) highlights that reactive power influences both voltage and frequency. But the connection between \( Q_L \) and \( f \) is crucial. In summary, a given \( Q_L \) will adjust frequency and a given \( P_L \) will adjust voltage.

![Figure 2.3: Single-phase model of a low-voltage grid that consists of a power-electronic generation unit and a linear \( RLC \) load. The system is islanded if the disconnection device is opened.](image-url)
Modelling the inverter control in synchronous reference frame, i.e. using the Park transformation, allows us to deduce per phase:

\[ P_{\text{inv}}(t) = \frac{1}{2} \cdot [V_d(t)i_d(t) + V_q(t)i_q(t)] = P_L(t) \]  
\[ (2.4) \]

\[ Q_{\text{inv}}(t) = \frac{1}{2} \cdot [-V_d(t)i_q(t) + V_q(t)i_d(t)] = Q_L(t) \]  
\[ (2.5) \]

where \( V_d \) and \( V_q \) are active and reactive part of the voltage respectively. Islanding voltage \( V_i \) can be calculated by using \( V_d \) and \( V_q \):

\[ V_i = \sqrt{V_d^2 + V_q^2} = \sqrt{2} \cdot V \]  
\[ (2.6) \]

\( V \) is the nominal RMS voltage. Under nominal conditions, \( V_i = \sqrt{2} \cdot V \approx 325 \text{ V} \).

A phase-locked loop (PLL) is used to control the reactive voltage \( V_q \) to zero. In steady state \( V_q(t) = 0 \). Thus \( V_d = \sqrt{2} \cdot V \) is constant over time too. With the basic concept of \( dq \) transformation that \( i_d \) and \( i_q \) are DC quantities in steady state operation and thus constant over time as well, (2.2)–(2.5) can be summarised to

\[ P_{\text{inv}} = \frac{1}{2} \cdot V_d i_d = \frac{1}{2} \cdot \frac{V_d^2}{R} \]  
\[ (2.7) \]

\[ Q_{\text{inv}} = -\frac{1}{2} \cdot V_d i_q = \frac{1}{2} \cdot V_d^2 \cdot \left( \frac{1}{2\pi f \cdot L} - 2\pi f \cdot C \right) \]  
\[ (2.8) \]

It can be further simplified to

\[ i_d = \frac{V_d}{R} \]  
\[ (2.9) \]

\[ i_q = -V_d \cdot \left( \frac{1}{2\pi f \cdot L} - 2\pi f \cdot C \right) \]  
\[ (2.10) \]

Equation (2.9) provides a clear expression between the control variable \( V_d \) and the actuating variable \( i_d \) considering the system gain \( R \). Thus, the voltage \( V_d \) in islanded grids can be controlled by the control of \( i_d \). This states that the voltage and active power are directly coupled in islanded grids consisting of inverters only. This is in contrast to the behaviour when connected to the transmission grid, when active power and frequency are coupled and reactive power and voltage are coupled.

In the following, the frequency behaviour will be analysed. For a capacitive load with negative reactive power \( Q_C = Q_L \), from (2.3) and (2.8) the following can be obtained:

\[ Q_C = -\frac{V_d^2 \cdot 2\pi f \cdot C}{2} = -\frac{1}{2} \cdot i_q \cdot V_d \]  
\[ (2.11) \]

It can be solved for \( 2\pi f = \omega \) and it is possible to get an expression that shows its dependency on \( i_q \). Composing the derivative shows that it is constant:

\[ \omega = \frac{1}{C \cdot V_d} \cdot i_q \]  
\[ (2.12) \]

\[ \frac{\delta \omega}{\delta i_q} = \frac{1}{C \cdot V_d} = K_{S,f,\text{cap}} = \text{const.} \]  
\[ (2.13) \]

Finally a clear expression between the control variable \( \omega \) and the actuating variable \( i_q \) is obtained.
Thus, the frequency $\omega$ in islanded grids with capacitive components can be controlled by the control of $i_q$. This states that frequency and reactive power are directly coupled in islanded grids consisting of inverters only. The investigation on inductive loads shows analogue results. For an inductive load with positive reactive power $Q_{\text{ind}} = Q_L$, from (2.3) and (2.8) the following is obtained:

$$Q_{\text{ind}} = \frac{V_d^2}{2 \cdot 2\pi f \cdot L} = -\frac{1}{2} \cdot i_q \cdot V_d$$  \hspace{1cm} (2.14)

It can be solved for $2\pi f = \omega$ and this results in an expression that shows the dependency on $i_q$.

$$\omega = -\frac{V_d}{L \cdot i_q}$$  \hspace{1cm} (2.15)

$$\frac{\delta \omega}{\delta i_q} = \frac{V_d}{L \cdot i_q^2}$$  \hspace{1cm} (2.16)

Thus $\omega$ depends on the inverse square of $i_q$ which makes the system nonlinear. But for a given $L$ under nominal conditions $\omega_n$, a Taylor expansion can be used for the nominal reactive current $i_{q,n} = \frac{V_d}{\omega_n \cdot L}$. From (2.8), the following is obtained:

$$\frac{\delta \omega}{\delta i_q} \bigg|_{\omega_n} = \frac{\omega_n^2 \cdot L}{V_d} = K_{S,f,\text{ind}}$$  \hspace{1cm} (2.17)

If $C$ is replaced with $-\frac{2Q_C}{\omega_n^2 \cdot V_d}$ from (2.11) and $Q_{\text{ind}} = \frac{V_d^2}{2\omega_n \cdot L}$ from (2.14) at nominal frequency, it can be seen that for the same absolute value of reactive power ($Q_{\text{ind}} = -Q_C$) it can be stated, that $K_{S,f,\text{cap}} = K_{S,f,\text{ind}} = K_{S,f}$.

$$K_{S,f,\text{cap}} = \frac{\delta \omega}{\delta i_q, C} = \frac{1}{C \cdot V_d} = \frac{\omega_n \cdot V_d^2}{-Q_C \cdot 2 \cdot V_d} = \frac{\omega_n \cdot V_d^2}{\frac{V_d^2}{2L \cdot \omega_n} \cdot 2 \cdot V_d} = \frac{\omega_n \cdot V_d^2}{V_d} = \frac{\omega_n \cdot L}{V_d} = \frac{\delta \omega}{\delta i_q, \text{ind}} = K_{S,f,\text{ind}} = K_{S,f}$$  \hspace{1cm} (2.18)

It can be seen that for the same amount of reactive power $Q_{\text{ind}}|_C$, the behaviour of both load types is almost equal with respect to changes of $i_q$ and because of this, (2.19) can be used to describe the frequency behaviour for both capacitive and inductive loads.

$$\omega(i_q) = \omega_n + K_{S,f} \cdot i_q$$  \hspace{1cm} (2.19)

**Figure 2.4** illustrates the frequency that results from a reactive current that deviates from its nominal value. It can be seen that both the inductive and the capacitive curve show almost the same behaviour at the nominal operating frequency 50 Hz.

Moreover, (2.19) shows that the larger $C$ or the smaller $L$, the lower is the gain $K_{S,f}$. Hence the changes in reactive current $i_q$ will result in a smaller frequency change. As the gain conditions vary and will be unknown under real conditions, an ordinary design for the frequency control loop is not appropriate. A new alternative approach will be shown in chapter 3.
Chapter 2. State of the Art

2.3.2 Influence of Nonlinear Loads

In the following, the effects of nonlinear loads will be outlined. This is based on the ZIP-model, which is a widely used modelling technique for composed loads in literature [25].

The ZIP-model

In [26], the effect of nonlinear loads on islanding detection methods of inverter based generation has been investigated. It was shown that there is a massive effect on islanding behaviour if a significant share of the loads cannot be modelled with a parallel $RLC$ load.

In fact the share of nonlinear loads is constantly increasing and therefore has been under investigation in grid simulation studies [23, 24, 27–29]. The modelling concept of nonlinear loads is based on the ZIP model which is defined and described as a general design rule in [25]. The ZIP model splits the load voltage behaviour into three terms, constant impedance ($Z$), constant current ($I$) and constant power ($P$):

$$P_L = P_n \cdot \left( a_Z \left( \frac{V}{V_n} \right)^2 + a_I \left( \frac{V}{V_n} \right)^I + a_P \left( \frac{V}{V_n} \right)^0 \right)$$ (2.20)

$P_n$ is the active power consumption under nominal voltage $V_n$. The parameters $a_{Z,I,P}$ can be used to construct a load model that consists of constant impedance, constant current and constant power parts respectively.

Electrical heating systems usually show a constant impedance behaviour. Examples are water heaters, boilers, ovens etc. Constant current loads were found to be an adequate model for the behaviour of compact fluorescent lamps [24]. Their influence on the overall low-voltage load behaviour has been on the increase. In the United Kingdom up to 20% of the loads are compact fluorescent lamps [27]. The standard use-case of constant power loads is a switch-mode power supply in electronic devices for example consumer electronics. In industry applications, frequency converters for electric drives are a common example for constant power loads.
2.3. Voltage and Frequency Behaviour in Islanded Grids

The ZIP model will be used in the following to express the behaviour of different load types in islanded grids and their effect on voltage stability. Therefore islanding voltage needs to be expressed as a function of the load composition.

**Power Equations for Different Load Compositions**

Constant impedance loads can be controlled relatively easy because they only evoke little change to the islanding RMS voltage $V$ when the active power $P$ changes:

$$ P = \frac{V^2}{R} \Rightarrow V = \sqrt{P \cdot R} \quad (2.21) $$

$$ \frac{\delta V}{\delta P} = \frac{\sqrt{R}}{2 \cdot \sqrt{P}} \quad (2.22) $$

Thus, voltage is a function of the square root of active power. The power consumption of constant current loads as a function of RMS voltage $V$ and RMS current $I$ is:

$$ P = V \cdot I \Rightarrow V = \frac{P}{I} \quad (2.23) $$

$$ \frac{\delta V}{\delta P} = \frac{1}{I} = \text{const.} \quad (2.24) $$

Hence, voltage changes are proportional to power changes. For constant power loads, the calculation of RMS voltage is trivial. The load will consume a constant power irrespective of the actual voltage level (in theory). Thus there is no stable operating point at a certain voltage and current level:

$$ \forall (V \cdot I) : (V \cdot I) = \text{const.} \quad (2.25) $$

$$ \frac{\delta V}{\delta P} \rightarrow \infty \quad (2.26) $$

The voltage behaviour of an unknown load composition will be described in the following. The total power $P$ consist of a constant impedance (linear load) term $P_Z$, a constant current term $P_I$ and a constant power term $P_P$:

$$ P = P_Z + P_I + P_P = a_Z \cdot P + a_I \cdot P + a_P \cdot P \quad (2.27) $$

$a_Z$ is the share of linear loads, $a_I$ is the share of constant current loads and $a_P$ is the share of constant power loads. $a_Z, a_I, a_P \in [0, 1]$ and $a_Z + a_I + a_P = 1$. The total active power consumption $P$ is a function of the RMS voltage $V$, the constant impedance $Z$, the constant RMS current $I$ of the constant current load and the constant power $P_P$:

$$ P = \frac{V^2}{Z} + V \cdot I + P_P \quad (2.28) $$

If voltage deviates from nominal value $V_n$, the power consumption $P$ will also deviate from nominal value $P_n$. But $Z$ and $I$ will stay constant. Thus $Z$ and $I$ can be calculated from their
Chapter 2. State of the Art

Figure 2.5: Acceptable power changes as a function of voltage changes for different types of loads.

respective load consumption:

\[ Z = \frac{V_n^2}{P_Z} = \frac{V_n^2}{a_Z \cdot P} \]  
\( (2.29) \)

and \( I = \frac{P_I}{V_n} = \frac{a_I \cdot P}{V_n} \)  
\( (2.30) \)

Using (2.29) and (2.30) in (2.28) results in an equation that expresses active power as a function of actual voltage.

\[
P = \frac{V^2}{V_n^2} \cdot P_Z + \frac{V}{V_n} \cdot P_I + P_P = P_n \cdot \left( \frac{V^2}{V_n^2} \cdot a_Z + \frac{V}{V_n} \cdot a_I + a_P \right) 
\]  
\( (2.31) \)

Figure 2.5 shows a comparison for the three load types. For a given voltage change of 10% of the nominal value, varying power consumptions can be calculated. Whereas for linear loads the load can change its active power consumption for about 20% of the nominal value, constant current loads can only change by 10%. Constant power loads cannot provide an active power load adaptation at all, thus they are the worst-case for controlling islanding voltage.

In islanded grids, the inverter has to provide the amount of power that is consumed by the load. If the provided active power deviates from nominal value, the islanding voltage will change. Dependent on the load composition (\(a_{Z,I,P}\)), the maximum possible value of \(\Delta P_{\text{max}}\) from nominal value can be calculated that leads to a violation of given voltage limits \(V_{\min}\) and \(V_{\max}\), for example ±10%.

\[
\Delta P = P - P_n \Rightarrow \Delta P = \frac{P}{P_n} - 1 
\]  
\( (2.32) \)

\[
\frac{\Delta P}{P_n} = a_Z \cdot \left( \frac{V_{\min/\max}}{V_n} \right)^2 + a_I \cdot \left( \frac{V_{\min/\max}}{V_n} \right) + a_P - 1 
\]  
\( (2.33) \)

Figure 2.6 illustrates the results. The higher the share of constant power loads, the smaller \(\Delta P_{\text{max}}\). The light grey area marks a combination of constant power with linear loads (\(a_I = 0; \ a_Z + a_P = 1\)). The dark grey area marks a combination of constant power with constant current loads (\(a_Z = 0; \ a_I + a_P = 1\)).
The investigations in this section show that the composition of loads has a high impact on voltage control in islanded grids. Neglecting constant power loads would not consider the variations of real behaviour in low-voltage grids. Hence, for experimental validation constant power loads in combination with linear RLC loads were used. The behaviour of the constant current load is a combination of linear loads and constant power loads and hence is covered by the investigation of constant impedance and constant power loads.
2.4 Inverter Setup and Control Strategies

In this thesis, only symmetrical conditions are investigated. Simulation and experimental results are obtained using an IGBT two-level three-phase inverter hardware setup, which is shown in Figure 2.7 (a). In the following, the single-phase equivalent circuit of Figure 2.7 (b) is used. There is a wide range of possible control architectures and strategies for inverter-based generation units. The following subsections provide a possible classification that covers the majority of the most common control strategies for inverter-based generation.

2.4.1 Grid Feeding Inverter Control

First, the main control principles are shown. They cover the most common controller designs for current, voltage and frequency control loops.

Figure 2.8 shows the typical control concept of simple grid feeding inverters in synchronous reference frame. The most common filter concept is the \( LCL \) filter composed of an inverter side inductance \( L_i \), filter capacitance \( C_F \) and a grid side inductance \( L_g \). Sometimes, the grid side inductance is replaced with a transformer. Due to the \( LCL \) structure of the filter, the filter design requires a careful consideration of resonances. The resonance frequency must differ significantly from the PWM switching frequency and the current controller bandwidth \([30]\). Theoretically one voltage and one current measurement would be sufficient. The voltage is used for grid synchronisation with a phase-locked loop (PLL) which provides the phase for the transformation to synchronous reference frame.

When using the synchronous reference frame, natural frame variables are first transformed to stationary reference frame with the alpha-beta transformation which is also called Clarke transformation and then into the synchronous reference frame with the direct-quadrature-zero transformation, also called Park transformation. The variables can be transformed back into the natural \( abc \) frame with the inverse transformations. In the control diagrams, the \( abc-dq \) block and the \( dq-abc \) block include the alpha-beta transformation. The transformation matrices can be found in appendix A.

![Diagram](image-url)
If voltages and currents are transformed into the $dq$ system, simple PI-controllers can be used for the current control loop. Current reference values $i_{dq}^*$ are calculated using the $d$ component of the grid voltage $V_d$.

The reference values for active power $P^*$ usually is provided by a DC-link control which tries to maximise the power output of the primary energy source—for example solar cell—with a so-called maximum power point tracking algorithm (MPPT).

The reference value for the reactive power $Q^*$ is a degree of freedom, mostly independent of the primary energy source. In the past, inverters were operating with a constant power factor $\cos \varphi = 1$. This has changed since grid codes demanded for ancillary services. Most common in low-voltage grids, inverters operate with reactive power dependent on their active power which is the so-called $Q(P)$ control. In medium- and high-voltage grids, $Q(V)$ control is more common. In addition, there are still generators that receive a fixed $\cos \varphi$ from the grid operator. This set-point could be either inductive or capacitive.

The grid feeding inverter of Figure 2.8 will be used to emulate the behaviour of old stock inverter generation in low-voltage grids and the behaviour of non-controllable generation.

### 2.4.2 Grid Forming Inverter Control

Figure 2.9 shows a typical control concept of grid forming inverters in synchronous reference frame. The current control loop is analogue to the grid feeding unit, but the current reference values are provided by the voltage controller. Voltage reference values $V_d^*$ and $V_q^*$ can be provided externally. Normally, $V_q^* = V_g$ and $V_q^* = 0$ is chosen. There is no conventional PLL. The phase angle $\varphi$ is provided by an integration of a reference frequency $\omega^*$. 
Figure 2.9: Overview of a control concept of a grid forming inverter control.

The voltage control loop usually measures the voltage at the output filter capacitance $C_F$. This capacitance can be designed large in order to stabilise the output voltage and improve the output characteristics in case of transient load changes [31].

This type of inverter generally has a low output impedance [32]. Power sharing for multiple inverter operation depends on the output impedances of each inverter. The synchronisation of multiple generation units is challenging. In this case, the frequency reference value $\omega^*$ must not be fixed because this would not result in a synchronous parallel operation.

As the output voltage and frequency should be independent of the primary energy source availability, usually stable DC voltage sources such as fuel cells or batteries are used.

2.4.3 Grid Supporting Inverter Control

Grid supporting control approaches can either be implemented as current sources, as shown in Figure 2.10 or as voltage sources, as shown in Figure 2.11. In either case, the inverter tries to regulate amplitude $E^*$ and frequency $\omega^*$ of the grid voltage [32].

The grid supporting current source inverter of Figure 2.10 is similar to the grid feeding inverter. A PLL is used for grid synchronisation and power is fed into the grid with the current controller. Additionally, this generator type is able to regulate voltage and frequency by controlling active and reactive power injection. In this case, the initial reference values $P^*$ and $Q^*$ are manipulated by the droop control parameters $k_p$ and $k_q$ respectively.

The grid supporting voltage source inverter of Figure 2.11 is connected to the grid via a virtual impedance. This kind of inverter control can be used in grid-connected and island modes without the need for a grid forming unit. The droop control compares the measured active and reactive power $P$ and $Q$—which is calculated from grid currents and voltages—to the reference values $P^*$ and $Q^*$ respectively.
and \( Q^* \). Incorporating the droop control parameters \( k_p \) and \( k_q \), voltage frequency and amplitude can be controlled.

**Figure 2.10:** Overview of a control concept of a grid supporting inverter control as a current source, modified from [32]

**Figure 2.11:** Overview of a control concept of a grid supporting inverter control as a voltage source, modified from [32]
2.4.4 The Droop Control Method

The droop control method incorporates the control of output active and reactive power dependent on frequency and amplitude with a proportional controller. Most often, the relation between active power and frequency \( (P - \omega) \) and reactive power and voltage \( (Q - V) \) is used, as shown in Figure 2.12 (a). This originates from the behaviour of synchronous generators which slow down when there is a lack of active power and speed up when there is an excess of active power. Dependent on the line impedances, this behaviour is also mimicked in droop controlled inverters.

Nevertheless, this control method reflects the small-signal behaviour close to the nominal operating point. As shown in section 2.3, the large-signal behaviour for linear \( RLC \) loads is vice versa: \( P - V \) and \( Q - \omega \). In [33] and [34], a reverse droop control was presented using a resistive impedance in order to improve the power sharing for resistive grids, as shown in Figure 2.12 (b). But still, the design principles were based on the small-signal behaviour. Thus, the droop control is not suitable for zero-voltage conditions, because in this case the large-signal behaviour is crucial.

The droop control was proven to be an effective method for sharing active and reactive power between multiple generation units [32, 33, 35]. The method was improved to work in both resistive and inductive grids by incorporating the virtual impedance in the voltage control loop. Thus, most commonly the droop control is used to share active and reactive power between voltage sources. But still, in order to incorporate accurate power sharing, the number of design parameters is relatively high and thus the overall control structure is quite complex. This is not useful because one of the aims in this thesis is to enable a large variety of inverters to operate in islanding mode. Those inverters incorporate different nominal powers, control structures and filter components.

Another big drawback of the droop control concept is, that fluctuations in loads and generations lead to small deviations from the set-point. The droop controllers only have proportional terms and thus cannot drive back steady-state errors. Because of this, a secondary control—either

\[
\begin{align*}
\text{inductive impedance} & \quad \omega & \quad \omega_0 \\
(P_0, P) & \quad (Q_0, Q) \\
\text{resistive impedance} & \quad V & \quad V_0 \\
(P_0, P) & \quad (Q_0, Q)
\end{align*}
\]

\( \omega_0 \)

\( V_0 \)

\( \omega_0 \)

\( V_0 \)

Figure 2.12: Voltage and frequency droop control characteristics. (a): inductive virtual impedance for grids with a high \( X/R \) ratio, (b): resistive virtual impedance for grids with a low \( X/R \) ratio, from [32].
centralised or decentralised—is needed to eliminate steady-state errors. This depends on a reliable communication infrastructure [36–39]. Communication infrastructure might be affordable if the number of generation units is relatively small. But applying this concept in low-voltage grids might not be very economic because of the large number of generators and the associated high costs for communication lines.

### 2.4.5 Master-Slave Control Method

In a master-slave concept, the master acts as a voltage source inverter whereas slaves operate as controlled current source inverters. If the master fails, there will be transients. When this technique is used in uninterruptible power supply (UPS) systems, an outage of the master normally activates one of the other slaves which takes over the master’s role. In UPS systems, there are several concepts of how to choose the master unit: 1) the master is a fixed generation unit, 2) the master is chosen randomly, 3) the biggest generation unit is defined as the master. Consequently, master-slave concepts as described are only possible if there is a high-bandwidth communication link between the generation units [40–42]. Figure 2.13 (a) shows the general concept.

There are some variations in the master-slave concept. For instance in [43], slaves are operated as current sources that receive their reference values from a local load current measurement. This is shown in Figure 2.13 (b). The master is only used for voltage and frequency reference. In theory, this would be possible without any communication. But in case the master fails, the whole system collapses. Additionally, every load current needs to be measured by a Slave unit. Otherwise the master would have to supply enough power without the support of the Slaves.

In [44], single master operation (SMO) and multiple master operation (MMO) have been compared. SMO defines a single voltage reference unit. The other generation units operate with a constant active and reactive power reference value—provided by the master or a central control unit via communication link. The MMO concept uses multiple voltage references in parallel but each of them equipped with a droop characteristic. Thus, the MMO concept is in fact a droop control method.

![Figure 2.13: Master-slave control concepts: (a) master provides reference currents to slaves via communication link, (b) slave receives its reference current from a local load current measurement, modified from [40].](image)
2.5 Implementation of Low-Voltage Ride-Through

The capability to provide low-voltage ride-through (LVRT) means grid support in the event of voltage drops. It aims to avoid unintentional disconnection of large feed-in power which could cause a network collapse [45]. LVRT capability is not a new requirement. Discussions about and proposals for the conjoint implementation of LVRT have been made in [46]. But so far, LVRT and anti-islanding detection (AID) have had contradictory requirements. LVRT can be divided into two main types:

- Limited LVRT: the so-called zero-power or zero-current mode. In this case, the inverter remains connected to the grid but no current is injected. This is mainly used in medium-voltage grids and is likely to be extended to low-voltage grids, too.

- Full LVRT: dynamic grid support capability by reactive current injection. This approach is mainly used in high- and very-high voltage grids.

Initially, LVRT was designed for high- and extra high-voltage grids. But due to the strong increase of generators connected to the medium-voltage network, LVRT became more and more important. LVRT contains the following requirements. Generators

- must not disconnect from the network in the event of network faults within a given window period (both limited and full LVRT);

- shall support the network voltage during a network fault by feeding a reactive current into the network (full LVRT);

- must not extract from the medium-voltage network after fault clearance more inductive reactive power than prior to the occurrence of the fault (both limited and full LVRT).

Figure 2.14 shows the LVRT borderlines for synchronous generators (type-1) and all other generators (type-2) connected to the medium-voltage grid in Germany. As long as the lowest value of the three line-to-line voltages stays above the borderline, generators must not become unstable or disconnect. These requirements apply to single-phase, two-phase and three-phase short circuits.

![Figure 2.14: LVRT borderlines for generators connected to the medium-voltage grid. Type-1: synchronous generators, type-2: all other generators, usually power electronics. The y-axis is in relation to the agreed service voltage $U_c$, referring the lowest value of three line-to-line voltages, according to [45].](image-url)
2.6 Anti-Islanding Detection

Recently, there have been approaches to extend LVRT capability to low-voltage grids or to make proposals for reasonable modifications of the existing grid codes [47-50]. The number of generators in low-voltage grids has risen in the past. For example, in Germany, more than 1.5 million PV inverters are installed to the low-voltage network and most of them have a nominal power of less than 20 kW as shown in Figure 1.2.

In [48], general modifications for PV grid codes have been proposed and in [47], LVRT capability in low-voltage grids has been recommended. These recommendations will partly be transferred into German grid codes and hence will be a key issue for future grid support and system stability. Embedding intentional islanding operation must not be at the expense of the rest of the grid, in other words, must not undermine LVRT capability.

Figure 2.15 shows the proposed LVRT borderline that will become mandatory for type-2 generators in Germany connected to the low-voltage grid. It will be used as a reference for simulations and experimental validations in chapter 5.

Figure 2.15: Possible future LVRT borderline for inverter-based generation, proposed in [47]

2.6 Anti-Islanding Detection

The detection of unintentional islanding operation (anti-islanding detection, AID) has become an issue in distribution grids several years ago. As distributed generation has been on the increase, there were more and more grids that had an excess of power and could theoretically maintain operation even if they are disconnected from the rest of the utility grid. Photovoltaic power plants, connected to the grid with inverters, are the most common form of distributed generation in low-voltage grids and thus have the highest need for an effective AID. New standards have been implemented in order to ensure secure and reliable power generation in low-voltage areas without the risk of unintentional islanding. For example, the main standards for Germany with regard to islanding were VDE 0126, including its revision in 2006 [51]. It was replaced by VDE-AR-N 4105 in 2011 [52]. There are also international standards like the IEEE standard 1547 [53], the IEEE standard 929 [54] and the JETGR0003-4-1.0 in Japan [55]. A comparison of different guidelines regarding islanding is presented in [56]. It provides a detailed analysis of different approaches in grid codes. In [48], a detailed analysis of low-voltage grid codes is provided, comparing and evaluating international codes with regard to AID, ancillary services, efficiency and reliability.
Chapter 2. State of the Art

There are a lot of different approaches for effective AID methods which can be categorised into remote, local passive and local active methods. Categorisations of AID methods can be found in [57–60]. Due to high costs, remote methods such as power line communication or transfer trip scheme are hardly used. Nevertheless, literature is rich in investigations on remote methods [61–64].

In recent years, active methods have been the focus of research because more and more grid codes stipulate active methods for generators that are connected to the grid via power electronics. The effectiveness of methods can be judged by the size and shape of the so-called Non-Detection Zone (NDZ). The NDZ is the area of operation where AID fails. AID methods are thus often compared by their NDZs, as in [65–67].

Normally, NDZs are calculated from steady state conditions when a generator is connected to a parallel $RLC$ resonant circuit with resonant frequency $f_{res} = 50$ Hz. There are three ways of illustrating NDZs: the $\Delta P/\Delta Q$ plane, the $C_{norm}/L$ plane and the $f_{res}/Q_f$ plane. The $\Delta P/\Delta Q$ plane is used to illustrate active and reactive power balances in islanded grids as shown in Figure 2.16. It shows the operating points in which unintentional islanding is not detected by a simple monitoring of voltage and frequency.

On the contrary, if a valid intentional islanding operation shall be maintained, the generators in an island have to operate inside this NDZ. Otherwise frequency or voltage limits will exceed the limits which can lead to damages in electrical equipment.

In chapter 5, the slip mode frequency shift method (SMS) will be used for the investigations on grid compatibility. The SMS method is a local active and a so-called frequency shifting method and one of the most common state-of-the-art AID methods [58,68].

The SMS method changes the reactive power injection of the inverter by imposing a phase shift $\varphi_{SMS}$ in the PLL. This phase shift is dependent on the actual frequency $f$, the maximum phase shift $\varphi_{max}$, the middle frequency $f_m$ and the nominal frequency $f_n$.

$$\varphi_{SMS} = \varphi_{max} \cdot \sin \left( \frac{\pi}{2} \cdot \frac{f - f_n}{f_m - f_n} \right) \quad (2.34)$$

This phase shift inside the PLL makes the island unstable at nominal frequency. Figure 2.17 shows the principle. The inverter shifts away the frequency until the load phase shift $\varphi_{Load}$ is equal to the PLL phase shift $\varphi_{SMS}$ again. The frequency eventually exceeds the limits $f_{min}$ or $f_{max}$ and the system is shut down. This works as long as the stable operating points are outside
2.6. Anti-Islanding Detection

Figure 2.17: Principle of the slip mode frequency shift (SMS) method. The inverter shifts frequency from the unstable operating point OP\(_0\) to one of the stable operating points OP\(_1\) OP\(_2\), derived from [58].

Figure 2.18: Non-detection zone (NDZ) of the slip mode frequency shift (SMS) method in the \(f_{\text{res}}/Q_f\) plane.

the frequency limits. This depends on the quality factor \(Q_f\) of the load. Thus the NDZ for this method can be drawn in the \(f_{\text{res}}/Q_f\) plane, as shown in Figure 2.18. The stronger the phase shifting (\(\varphi_{\text{max}}\)), the smaller the NDZ.

In [69, 70], investigations have been done on the impacts of low-voltage grid codes on islanding behaviour of inverter-based generation. New effects have been discovered and quantified that explain how stabilisation in cases of unintentional islanding can occur due to ancillary services. Based on these results, new control approaches for intentional islanding operation have been developed and are proposed in chapter 4.

Necessary changes in AID for a successful islanding operation

When intentional islanding operation as proposed in this thesis is implemented, the standard AID mechanisms require modification. Obviously, the inverters that try to operate in a stable island must deactivate their active AID methods. This means that there is no intentional
slip mode frequency shifting during islanding operation because this would undermine a stable control loop.

In the beginning, islanding will be initiated from zero-voltage condition. Thus, voltage and frequency violations must not cause a shut-down of the inverter whilst it is still trying to establish nominal voltage and frequency. Instead, there must be a window period meanwhile the inverter has time to operate at nominal voltage and frequency. After the window period has expired, AID must be re-activated to the effect that voltage and frequency violations lead to tripping in accordance with the grid codes. But still, active AID methods such as slip mode frequency shifting must remain deactivated.
Chapter 3

Modelling and New Controller Design for Single Inverter Operation

In this chapter, a new voltage and frequency control design procedure for islanding operation will be presented which can be applied to inverters irrespective of the underlying filter design, the current controllers or additional points of measurement. Voltage and frequency will be controlled independent of the actual load conditions and the current control loop. After the design procedure, the control loops are analysed in simulations with regard to their effectiveness for linear and nonlinear loads. The scalability of the method is shown and subsequently control robustness and control stability will be investigated using Bode and Nyquist analysis. Finally, experimental tests in the lab demonstrate islanding operation for linear loads and nonlinear constant power loads.

3.1 Requirements and New Control Concept

Figure 3.1 (a) shows a single-phase equivalent circuit of an ordinary grid feeding unit (see also section 2.4). In both simulation and experimental results, a two-level three-phase inverter system is used. It receives its reference values $i^*$ from an integrated power controller (most often an MPPT algorithm). Several measurement points for current and voltage might be required for the current control loop which provides the modulation signals for the PWM generation that drives the power electronic switches. The inverter in Figure 3.1 (a) is not able to provide islanding operation. Therefore, it needs to be transformed into a grid forming unit.

Existing design methods for grid forming inverters use holistic approaches. This means, that if an inverter is intended to be used in islanding operation, this is already considered in the hardware design. Often, a relatively large filter capacitance is used [31]. Advanced methods measure the grid side current and provide it to the control loop as a feed-forward signal or only local loads can be supplied because its current must be measured [71, 72]. These limitations also apply to so-called unified control approaches [73, 74]. Of course, the benefit of the state-of-the-art approaches is that the whole control loops are optimised for the actual islanding conditions and thus provide a high level of controllability and voltage and frequency quality. But none of the specialised technologies can be used without considering details of the filter or transformer design, details of the current control loop or with the usage of only one current and one voltage measurement.

Thus, a possible solution for islanding operation in low-voltage grids would be to use only inverters that were designed for this purpose. But this might not be very reasonable because a lot of potential that is already available as old stock inverters would remain unused. Besides, if every inverter has its specific design, it cannot be ensured that the operation of multiple inverters
in parallel would result in a stable control. Furthermore, every generation unit which is not part of a common control concept might become an additional disturbance for those inverters that try to maintain islanding operation.

Hence, a design method is required that can be used for various inverters irrespective of their hardware characteristics, the underlying current control loop and measurements. Another challenge is to show that this unified controller design is able to operate islands over a wide range of different load conditions without being able to gather any information on the loads.

Thus, a new controller design concept will be presented to overcome the drawbacks of the state-of-the-art approaches. Figure 3.1 (b) illustrates the new control concept that is developed in this thesis (dark-grey box) and the two challenges (light-grey boxes) that have been overcome with the new controller design concept: 1) unknown inverter hardware and control and 2) unknown load conditions with a value below the inverter’s nominal power.

During grid parallel operation, the system works as a simple grid feeding unit with the aim to inject maximum power. The new control has no effect during grid parallel operation. During islanding operation, the inverter is enhanced with the newly designed voltage and frequency control. It is not aiming to inject a maximum of power any more. The voltage $V$ and frequency $\omega$ will now be controlled independent of the actual load conditions and the current control loop. This is incorporated by a voltage measurement. As voltage also must be measured for grid parallel operation, no additional point of measurement is required.

The new design procedure will be presented in the following. It only requires the inner current control time constant $\tau_i$ and the inverter nominal power $P_n$. Theoretically the time constant $\tau_i$ could be even estimated and still the method works as will be shown later.
3.2 Voltage and Frequency Control Loop Design

Figure 3.2 shows the new voltage and frequency control structure including the feed-forward admittances which is proposed in this thesis. The light grey parts are analogue to the ordinary grid feeding unit of section 2.4. The dark grey parts are newly added and contain a voltage control loop, a frequency control loop and virtual admittance feed-forward signals. Details on the proposed controllers will be explained in the following subsections.

The equivalent circuit for the inverter consists of a current and voltage measurement and a filter unit. Many advanced control strategies use multiple current and/or voltage measurements to include feed-forward signals into their control structure, e.g. inverter- and grid-side current in topologies with LCL filter. But the proposed design method shall be independent and universally usable for a big variety of underlying inverter structure and design. As indicated in Figure 3.1 (b), the voltage and frequency control loops are designed to be independent of the underlying current controller and even measurement points. For both voltage and frequency control loop, only the grid-side voltage is required. It must be measured anyway in controlled inverter systems. Thus it can be concluded, that no additional hardware should be required to incorporate the proposed control method if the processing power of the controller implementation is neglected.

Of course, in order to establish islanding operation, the anti-islanding detection (AID) of the inverters need to be deactivated. In case the state-of-the-art slip mode frequency shift algorithm is used, the phase shift \( \phi_{\text{SMS}} \) needs to be set to zero. Furthermore the inverter tripping due to over- and under-voltage must also be deactivated. Otherwise the inverter would not start injecting power from zero-voltage condition.

---

Figure 3.2: General control approach of the new controller design. The dark grey boxes contain the new voltage and frequency control loops incorporating the virtual admittances which are designed in the following sections.
3.2.1 State-of-the-Art Current Control Loop

For a general validation of the concept, a basic current controller in the synchronous reference frame is used. Details on the designing method can be found in [75] and [69]. In order to separate the behaviour of the $d$ and $q$ components respectively, a state-of-the-art dynamic decoupling like in [75] is used. This allows to analyse $d$ and $q$ current control separately and to use the equations that have been derived in section 2.3.

In [75], the current controller is designed with a dynamic compensation of the used $L$-filter. The normal hardware architecture that is used in grid connected inverters is an $LCL$ filter. Thus, the design concept requires slight adaptation. By neglecting the influence of the filter capacitance $C_F$ in steady state and assuming that $L_F = L_i + L_g$ and $R_F = R_i + R_g$, the dynamic decoupling can be implemented as in [75]. The transfer function of the $LCL$ filter, which is of third order, can be simplified to a first order system as for a simple $L$ filter. A comparison of the transfer functions for an $L$ and an $LCL$ filter is provided in Appendix B. Like in [75], a suitable design of the current controller can be done by compensating the filter time constant $T_1 = \frac{L_F}{R_F}$ in the open-loop transfer function $F_0(s)$ with the controller time constant $T_N$:

$$F_0(s) = \frac{1}{1 + \frac{1}{T_1} \cdot s} \cdot \frac{K_P (1 + T_N \cdot s)}{T_N \cdot s} = \frac{K_S K_P}{T_N \cdot s}$$  \hspace{1cm} (3.1)

With $K_S = \frac{1}{T_1}$ as the system gain and $K_P$ and $T_N$ as the design parameters of the current controller. This results in a closed-loop transfer function $F_{W,C}$ of a simple first order system with the design parameter $\tau_i$, that can be adapted with a suitable $K_P$:

$$F_{W,C}(s) = \frac{F_0(s)}{1 + F_0(s)} = \frac{1}{1 + \frac{1}{T_S/K_P} \cdot s} = \frac{1}{1 + \tau_i \cdot s}.$$  \hspace{1cm} (3.2)

With this, the inner current control loop is designed properly, which means its transfer function can be approximated by a first order system with the time constant $\tau_i$. Thus, outer control loops can assume the transfer function between the reference currents and actual currents to be of first order behaviour. This is only valid if the time constants for outer control loops are significantly larger.

As mentioned in the beginning of chapter 2, there are also different approaches of designing the inner current control loop such as using a proportional resonant controller (PR) in stationary reference frame [76–78]. In some aspects, the PR controller has some advantages over the PI controller design in synchronous reference frame, for example with respect to harmonic compensation [79,80]. But it also has some disadvantages when it comes to varying frequencies because normally it is tuned to nominal frequency. Although there are countermeasures against that such as an adaptive adjustment of the controller frequency [81]. In summary there are manifold current controller design approaches with pros and cons, but as the focus in this thesis is not on the current controller design, a very simple design in synchronous reference frame seems appropriate. If the current controller is designed in stationary reference frame, the $dq$ reference values can be transformed using the inverse Park transformation as shown in appendix A.

3.2.2 New Voltage Control Loop Design

Having designed the current control loop with a state-of-the-art approach, the new voltage and frequency controls can be implemented. In islanded grids, the steady state voltage level results
from a balance between generation and consumption of active power. With the inverter control applied in synchronous reference frame and a phase-locked loop (PLL) driving $V_q$ to zero, the islanding voltage $V_i$ amounts to

$$V_i = \sqrt{V_d^2 + V_q^2} \approx V_d \tag{3.3}$$

$V_d$ only depends on the active current $i_d$. This simplifies the control of $V_d$ to the control of a suitable current reference value $i_d^*$, which is then tracked by the inner current controller.

Figure 3.3 shows the overall control structure for the new voltage controller design, which consists of the inner current control loop, a virtual feed-forward admittance $R_{\text{ff}}^{-1}$ and a PI controller for the voltage control loop. The structure itself is not new as the concept of virtual admittance was used in [31]. But in [31], the design method is limited to $LC$ filters with a large grid side capacitance. Thus the controller design that was presented in [31] cannot be used irrespective of the filter design.

However, the concept of virtual admittance is helpful if the actual load conditions are unknown. It is used to make the voltage control loop stable irrespective of the actual load conditions. Figure 3.2 shows the resistor $R_{\text{ff}}$ in the equivalent circuit of the inverter connected to a local load $R_L$. With the design of $R_{\text{ff}}$, the system can be sufficiently damped, irrespective of the actual load demand. However, $R_{\text{ff}}$ is not an actual damping resistor because it is only used virtually.

But to make the method usable for various inverter hardware setups, a new controller design method must be developed which is presented in the following. The overall transfer function of the new voltage control loop $F_{W,V}(s)$ amounts to:

$$F_{W,V}(s) = \frac{V_d}{V_d}(s) = \left( \frac{1}{R_{\text{ff}}} + \frac{1}{R_L} - \frac{1}{F_{\text{CC}}} + \frac{1}{F_{\text{CC}}F_{\text{PWM}}} \right)$$

$$\quad + \frac{1}{F_{L_{\text{d}}}F_{\text{CF}}F_{\text{CC}}F_{\text{PWM}}} + \frac{F_{L_{\text{g}}} + F_{L_{\text{d}}} + \frac{1}{F_{\text{CF}}}}{R_L \cdot F_{L_{\text{d}}}F_{L_{\text{g}}}F_{\text{CC}}F_{\text{PWM}}} \right)^{-1} \tag{3.4}$$

Where $F_{L_{\text{d}}}$ and $F_{L_{\text{g}}}$ are inverter and grid side inductors, $F_{\text{CF}}$ is the filter capacitor, $F_{\text{CC}}$ is the current controller and $F_{\text{PWM}}$ is the PWM generation, which is approximated by a first order system with time constant $\tau_{\text{PWM}} = 1.5 \ T_s$, with $T_s$ as the sampling time. It can be seen that the overall transfer function is characterised by the terms $\frac{1}{R_{\text{ff}}}$ and $\frac{1}{R_L}$. Together, these parts represent a parallel circuit of the actual load $R_L$ and the virtual load $R_{\text{ff}}$. If $R_{\text{ff}}$ is chosen properly, the system can be designed stable for all relevant load conditions $R_L$.

For the new design process, suitable simplifications of the transfer function are met that still provide a proper description of the system but require only a minimum amount of values of the
Figure 3.4: Simplified voltage control loop: (a) inner current controller as a first order system, (b) rearrangement of (a) for simple PI design procedure. Cross-coupling of the d and q component is neglected in this figure.

existing inverter: the current controller time constant $\tau_i$ and the inverter nominal power $P_n$.

The new voltage control loop design of Figure 3.3 offers three design parameters: proportional and integral term of the PI controller and the virtual feed-forward admittance $R_{ff}^{-1}$. First, a suitable value for the feed-forward admittance needs to be defined. By using the base impedance $Z_{Base}$, the value is intrinsically adapted to the inverter size. The base impedance can be derived from the nominal power and voltage of the inverter:

$$Z_{Base} = \frac{V_{Base}}{I_{Base}} = \frac{3 \cdot V_d^2}{2 \cdot P_n} \quad (3.5)$$

A proper damping of the system can be maintained if the feed-forward admittance is set to three times the base impedance. This means, that the inverter is exposed to a virtual load that is at least one third of its nominal power. This alleviates control stability problems for small load conditions that have little damping.

Second, the proportional and integral terms of the PI controller are designed. In order to simplify the control loop design process, the current control loop is assumed as a first order system like shown in Figure 3.4 (a). With re-arranging the block diagram, the structure can be simplified to a first order system with gain $K_{S,V}$ and time constant $\tau'$ as shown in Figure 3.4 (b):

$$K_{S,V} = \frac{1}{R_{ff}}$$

$$K_{S,V} = \frac{1}{(1 + \frac{R_{ff}}{R_L}) \cdot \tau_i \cdot s}$$

$$K_{S,V} = \frac{1}{(1 + \frac{R_{ff}}{R_L} + \frac{R_{ff}}{R_{eff}}) \cdot \tau_i \cdot s} = \frac{1}{(1 + \tau' \cdot s)}$$

$K_{S,V}$ depends on the actual load conditions $R_L$, which are unknown. But there are two restrictions that limit $R_L$ and thus $K_{S,V}$. The first is $R_L \rightarrow \infty$. In this case, $K_{S,V}$ is dominated by $R_{ff}$. The other restriction is the maximum power the inverter can provide because islanding
3.2 Voltage and Frequency Control Loop Design

The step response of the plant model $F_{SV}(s)$, which is the open loop voltage transfer function including the feed-forward impedance $R_{ff}$, low (solid) and high (dashed) load conditions and simplification (dotted line) for the worst-case condition with a first order system with $\tau' = 2 \cdot \tau_i$.

The maximum amount of the inverter’s active power is consumed at $R_L = Z_{Base}$, thus it states, that

$$R_L \geq Z_{Base}.$$  

The two restrictions can be used to define a range for $K_{SV}$:

$$K_{SV} = \frac{R_L \cdot R_{ff}}{R_L + R_{ff}} \Rightarrow \frac{3}{4} \cdot Z_{Base} < K_{SV} < R_{ff} = 3 \cdot Z_{Base}$$  \hspace{1cm} (3.7)

This limitation allows to design the voltage controller $F_{VC}(s)$:

$$F_{VC}(s) = \frac{K_{PV} \cdot (1 + T_{NV} \cdot s)}{T_{NV} \cdot s}$$  \hspace{1cm} (3.8)

Because $F_{SV}(s)$ is approximated with a first order system, dynamic compensation with $T_{NV} = \tau'$ can be used. The open $F_{0,SV}(s)$ and closed-loop $F_{W,SV}(s)$ transfer function for the voltage control can be derived.

$$F_{0,SV}(s) = \frac{K_{SV}}{(1 + \tau'_i \cdot s)} \cdot \frac{K_{PV} \cdot (1 + T_{NV} \cdot s)}{T_{NV} \cdot s} \approx \frac{K_{PV} \cdot K_{SV}}{T_{NV} \cdot s}$$  \hspace{1cm} (3.9)

$$F_{W,SV}(s) = \frac{1}{1 + \frac{1}{F_{0,SV}(s)}} \approx \frac{1}{1 + \frac{T_{NV}}{K_{PV} \cdot K_{SV}} \cdot s} = \frac{1}{1 + \tau_V \cdot s}$$  \hspace{1cm} (3.10)

Thus, the designed voltage control loop will nearly show a first order system behaviour with the time constant $\tau_V$ as long as the simplification of the current control is valid.

Finally, $\tau_V$ can be designed by choosing $K_{PV}$. As a general design rule for cascade control architectures, the outer control loop should be designed slower than the inner control loop. Thus,
the voltage control time constant should be larger than the current control time constant. In the following, the new controller design procedure will be investigated with a relatively challenging small time constant of $\tau_V = 4$ ms, which is only twice the current control time constant.

Figure 3.6 shows the closed loop step response of the overall voltage control loop with $\tau_1 = 2$ ms for two possible time constants $\tau_V$ and for $R_L = \left[Z_{\text{base}}, \infty\right]$. The larger $R_L$, the steeper the step response. As it can be seen, even under open circuit conditions and $\tau_V = 4$ ms, the control loop quickly reaches its reference value and only with a small overshoot.

### 3.2.3 New Frequency Control Loop Design

In literature, islanding operation is often realised by fixing frequency at the nominal value. This is also illustrated for the state-of-the-art grid feeding inverter in section 2.4. Instead of controlling it via reactive power, the phase-locked loop (PLL) gets a constant frequency as an input. The advantage of this method is, that there is no need for a frequency control loop. But then it would be challenging if the inverter was not able to provide enough reactive power for the connected loads. In addition, there are more disadvantages when it comes to multiple inverter operation. Multiple inverters must be able to synchronise. This is not possible if every generation unit has its own fixed reference frequency.

Because of this, a new design concept for the frequency control loop is proposed in the following, using a direct control of the reactive current rather than operating with fixed frequency. Therefore, the conventional PLL of the grid feeding unit must be integrated into the frequency control concept.

**Phase-Locked Loop**

The newly proposed frequency control uses a conventional PLL, which is the synchronisation component in grid parallel operation. A possible design of the PLL is shown in Figure 3.7. Its development was not part of this work. Reference [75] provides a standard design procedure for PLLs. The relevant parameters are provided in Table 3.1. The PLL incorporates an integral
3.2. Voltage and Frequency Control Loop Design

The term \( \left( \frac{h}{s} \right) \) that drives the \( q \) component of the voltage \( V_q \) to zero. The measured frequency \( \omega \) is provided for the frequency control loop. The actual design of the PLL can vary strongly, dependent on the desired dynamics and design targets. Thus it is not easy to generalise the frequency behaviour for different PLL approaches. The integral term eventually drives \( V_q \) to zero, hence the task of frequency control has to focus on transient stability and setting of the desired value \( f = 50 \) Hz. A general design constraint for PLLs of grid feeding inverters is that frequency changes are relatively small due to the large inertia of the utility grid. In fact, a fast responding PLL could undermine the control stability of grid-feeding inverters. Thus, it can be concluded that the PLL probably would not be able to control \( V_q \) to zero during fast transients.

For the implementation of the proposed frequency control in this thesis, the PLL was changed in a single point. During the start-up process of islanding operation, the system faces high frequency transients. In order to overcome this, the PLL is fixed with a saturation block during the start-up as shown in Figure 3.7. This allows to avoid forbidden frequencies that exceed the limits of 47.5 Hz and 51.5 Hz. After 200 ms, the system is in steady-state and the frequency limitation of the PLL is deactivated.

**General Approach**

For the frequency controller design the necessary amount of reactive power \( |Q_{RLC}| \) needs to be considered. The main problem is that theoretically \( |Q_{RLC}| \) can vary within the range of \( P_n \). This is the maximum amount of reactive power, the inverter could provide. Thus, using a conventional PI controller is not suitable and another advanced control method has to be used which is introduced in the following.

In islanded grids, frequency changes can be much higher than in grid parallel operation. Even more important, frequency is not decoupled from inverter current injection. In fact, the inverter

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \omega_c )</td>
<td>Bandwidth of the PLL</td>
<td>150 rad</td>
</tr>
<tr>
<td>( p )</td>
<td>Design parameter of the lead compensators</td>
<td>( \omega_c \cdot \sqrt{\alpha} )</td>
</tr>
<tr>
<td>( \alpha )</td>
<td>Design parameter of the lead compensators</td>
<td>( \frac{1+\sin(\delta_m)}{1-\sin(\delta_m)} )</td>
</tr>
<tr>
<td>( \delta_m )</td>
<td>Phase shift of the two lead compensator</td>
<td>45°</td>
</tr>
<tr>
<td>( h )</td>
<td>PLL integrator gain</td>
<td>( 1.47 \cdot 10^5 ) V(^{-1} )</td>
</tr>
<tr>
<td>( \omega_0 )</td>
<td>Nominal frequency</td>
<td>314 rad</td>
</tr>
</tbody>
</table>
current is the main reason for the frequency behaviour. If grid voltage depends on the actual current feed of the inverter itself, \( V_q = 0 \) does not hold true during transients. If \( dq \) currents are fed into the grid and the PLL is no more able to drive \( V_q \) to zero, \( V_d \) and the active power are not only dependent on \( i_d \) anymore and the reactive power is not only dependent on \( i_q \) either. As long as the reactive current consumption of the load does not match reactive current generation of the inverter, \( V_q \) will not be zero.

Figure 3.8 shows a model of the \( q \) component of the voltage. The reactive current \( i_q \), the inverter has to provide, depends on the actual frequency \( \omega \), the inductive or capacitive impedance of the load \( X_{C,L} \), and the islanding voltage \( V_i \) which is approximately \( V_d \). The actual demand of the load for reactive current \( i_q^\sim \) can be seen as a disturbance input which drives \( V_q \neq 0 \) and depends on the absolute value of \( X_{C,L} \). For inductive loads, \( X_{C,L} > 0 \) and thus \( i_q^\sim > 0 \) and vice versa.

The proposed solution that is used in the frequency controller to enhance the frequency behaviour of the islanding inverter is the usage of \( V_q \) as a feed-forward signal for the injection of reactive current \( i_q \). This concept has been integrated into the plant model as shown in Figure 3.8.

**Fast Frequency Response**

Because of the relatively slow disturbance reaction of conventional PLLs, the newly proposed frequency control loop adds two more parts: 1) a fast responding part and 2) a relatively slow part to reach the nominal frequency value in the long run.

The controller of Figure 3.8 is composed of two parts: an integrator for the frequency deviation from nominal value and the feed-forward signal from the reactive voltage \( V_q \), which provides a fast response as an addition to the PLL. If \( V_q > 0 \), the islanded system lacks of positive reactive power to operate in a stable point, thus additional negative reactive current has to be provided and vice versa.

First, the feed-forward gain \( X_{ff}^{-1} \) needs to be designed. Due to its power ratings, the inverter is only capable of providing a certain amount of active and reactive power \( Q_{\max} \), which is the nominal power \( P_n \) of the inverter. Thus its per phase reactive current limit \( i_{q,\max} \) amounts to:

\[
i_{q,\max} = \frac{2 \cdot Q_{\max}}{3 \cdot V_{d,n} \cdot B_{\text{Base}}} = \frac{V_{d,n}}{Z_{\text{Base}}}
\] (3.11)
3.2. Voltage and Frequency Control Loop Design

where \( V_{d,n} \) is the nominal value of \( V_d \). As explained previously, \( V_q \) will deviate from zero and thus the actual phase of the island and the phase that is measured by the PLL are not aligned. In order to operate the control system in a linear small signal setting, the deviation between the actual phase of the island and the phase of the PLL needs to be small so that it states: \( \sin(\Delta \omega t) \approx \Delta \omega t \). In other words, \( V_q \) must not exceed a certain limit of \( \pm V_{q,\text{max}} \). \( X_{ff}^{-1} \) can be calculated from:

\[
X_{ff} = \frac{V_{q,\text{max}}}{i_{q,\text{max}}} = \frac{V_{q,\text{max}}}{V_{d,n}} \cdot Z_{\text{Base}} \tag{3.12}
\]

A reasonable value is \( X_{ff} = \frac{1}{4} Z_{\text{Base}} \). This means, that as soon as \( V_q \) reaches \( \frac{1}{4} \cdot V_{d,n} \), the maximum amount of reactive current \( i_q \) is injected by the inverter and immediately drives back \( V_q \) to zero. Thereby, a linearisation with a maximum error of about 1.04% is obtained:

\[
\sin(\Delta \omega t)|_{\Delta \omega t=0.25} = 0.2474 \Rightarrow \frac{\sin(\Delta \omega t)}{\Delta \omega t}|_{\Delta \omega t=0.25} = 0.9896 \Rightarrow 1.04\% \text{ error} \tag{3.13}
\]

\( \Delta \omega t = 0.25 \) equals a phase angle of 14.3°. Thus, a misalignment of the PLL and the actual islanding voltage of 14.3° results in an injection of the maximum reactive current.

If \( X_{ff} \) is chosen smaller, the deviation of \( V_q \) will be even lower, but this comes along with a very strong noise of the reference value of \( i_q \), thus there has to be a reasonable compromise. In combination with the integral term of the PLL, the feed-forward admittance \( X_{ff}^{-1} \) ensures a good tracking performance of the frequency and zero steady-state error for \( V_q \). As the PLL has some time constants and it is still a nonlinear part of the overall control system, there will be some transient effects in the frequency control.

**Long Term Frequency Control**

The provision of reactive power using a feed-forward loop gives a fast response of the current controller to provide a certain amount of reactive current, which is necessary to operate around a certain frequency and to keep \( V_q \) close to zero. But this frequency has to be controlled to nominal 50 Hz with zero steady-state error. To obtain this, the newly proposed control design also includes an integral term as shown in Figure 3.8.

According to (2.10) and (2.19) in section 2.3, the relation between reactive current and frequency can be linearised around nominal frequency. This means, that a deviation of \( \Delta f = 1 \) Hz results from a 2% error in reactive current. The design goal for the integral term of the frequency controller is to reduce this error to a certain level within a certain amount of time.

Due to the nearly linear behaviour inside 47.5 Hz and 51.5 Hz, the closed loop transfer function of the integrator can be estimated by a first order system with time constant \( \tau_i \). The PLL frequency is limited to 47.5...51.5 Hz during the transient start-up process. Thus, the maximum frequency deviations can be calculated to:

\[
f(t) = \begin{cases} 
47.5 \text{ Hz} + 2.5 \text{ Hz} \left( 1 - e^{-\frac{t}{\tau_i}} \right) & \text{for capacitive loads} \\
51.5 \text{ Hz} - 1.5 \text{ Hz} \left( 1 - e^{-\frac{t}{\tau_i}} \right) & \text{for inductive loads}
\end{cases} \tag{3.14}
\]
A good frequency response can be obtained if the frequency deviation error $\Delta f$ is reduced to below 1% within $t_{\text{max}}$:

$$|1 - e^{-\frac{t_{\text{max}}}{\tau_f}}| \geq 0.99 \Rightarrow -\frac{t_{\text{max}}}{\tau_f} \geq \ln(0.01)$$

$$\Rightarrow \tau_f \leq \frac{t_{\text{max}}}{\ln(0.01)} \quad (3.16)$$

The exponential function of a first order system reaches 99% of the final value within $t_{\text{max}}$. This is about five times the time constant $\tau_f$. Thus for reaching nominal value within 100 ms, $\tau_f$ can be designed to 20 ms. This is shown in Figure 3.9.

During the start-up process, there will be a maximum frequency deviation that is limited by the saturation of the PLL: 47.5–51.5 Hz. This input deviation of the nominal frequency $\Delta f_{\text{max}} = 1.5-2.5$ Hz must lead to a reference reactive current $i_{q,\text{max}}$. The maximum amount of reactive current that can be provided by the inverter $i_{q,\text{max}}$ can be calculated by its power ratings $P_n$. Realistic load conditions normally have a higher active power demand than reactive power demand. Their load quality factor is usually below 0.5. Thus, large loads with $P_L = P_n$ will most likely consume less than 0.5 $P_n$ reactive power. Hence, the demand for reactive current is also halved.

When the nominal frequency has to be reached within $t_{\text{max}}$, the integral gain $K_{I,f}$ can be derived with

$$K_{I,f} = \frac{1}{1.5/2.5 \text{ Hz}} \cdot \frac{1}{\tau_f} \cdot 0.5 \cdot i_{q,\text{max}}$$

If $K_{I,f}$ follows (3.17), the relevant reactive loads can be sufficiently supplied by the inverter reactive current within $t = 100$ ms.
3.3 Simulation Results

In the following, the proposed control strategy is validated by simulation. Islanding behaviour strongly depends on the type of loads that it is composed of. Hence, tests with both linear and nonlinear loads are executed.

3.3.1 Operation with Linear Loads

In Figure 3.10, the setup for simulation and experimental results with linear loads is shown. The parallel resonant circuit is parametrised for relevant active, inductive reactive and capacitive reactive power combinations. This represents the sample space in which the inverter’s behaviour is demonstrated. The following results show the voltage at the terminals of the device under test.

Figure 3.11 shows the step response of the voltage control loop for several active load conditions \(Q = 0\). The grey area illustrates the expected range of the step response which depends on the actual load conditions. The step response of Figure 3.11 shows that in simulation, the islanding behaviour is in accordance with the predictions of the modelling process. The nominal
value can be reached within less than 100 ms. In open circuit conditions ($P = 0$), there is a 10% overshoot for about half the fundamental period.

Figure 3.12 shows the step response of the voltage control loop for several resistive-reactive load conditions. The reactive power was set to half of the nominal power of the inverter, which is a relatively high value. In case of a damped system ($P = P_n$), both inductive and capacitive curves almost match the model. The quality factor $Q_f$ in this case is 0.5. With a low damping ($P = 0.1 P_n$ and $Q_f = 5$), there is an overshoot of about 10% for capacitive and 20% for inductive loads. This overshoot results from the fact that the voltage components $V_d$ and $V_q$ are dynamically coupled. In the design process, no decoupling was implemented because the coupling depends on the filter capacitor which is assumed to be unknown.

Figure 3.13 shows the disturbance reaction of the frequency control loop for different purely active load conditions at the time when the inverter rebuilds the voltage. In the beginning, the frequency faces a disturbance and thus it deviates from nominal value. The lower the damping, the bigger the deviation. The control loop is able to reach the nominal value within 100 ms.

Figure 3.14 shows the disturbance reaction of the frequency control loop for several active and reactive load conditions. In case the load is inductive, the frequency first increases but can be restored within 50 ms. In case the load is capacitive, the frequency first drops to the lower limit of 47.5 Hz where it is fixed by the inverter’s PLL. The reactive current is increased further and finally frequency can be restored within 100 ms.

In summary, the simulation results match the model predictions for the investigated load conditions. In case the active load is actually larger than the inverter nominal power, the inverter is not able to reach the nominal voltage. Thus the increase of the voltage would be flattened. However, the control would still be stable because the damping of the system improves if the load is even larger. In case the reactive power is larger than the nominal power of the inverter, the transient frequency deviations increase and the saturation of the PLL might cause problems for the integral term of the frequency control loop. In this case, it would take longer to control frequency to nominal value. Besides, the current limitations of the inverter could also effect the voltage control loop because the reactive current has priority over the active current.
3.3. Simulation Results

Figure 3.13: Simulation validation with linear RLC load. Disturbance reaction of the frequency control loop for several resistive load conditions.

Figure 3.14: Simulation validation with linear RLC load. Disturbance reaction of the frequency control loop for several resistive-reactive load conditions.

3.3.2 Operation with Nonlinear Loads

Figure 3.15 shows the setup for simulation and experimental tests with nonlinear constant power loads (CPL). For the CPL, a controlled rectifier is used. The following results show the voltage at the terminals of the device under test.

Figure 3.16 shows the results for an islanding operation with a controlled rectifier as a CPL. Starting from a zero-voltage condition, the inverter starts to increase voltage in the island. Due to the large DC capacitance of the CPL, there is a short overshoot of about one fundamental period. Due to the high level of harmonics in the system, the control faces non-constant dq variables. After the pre-charging of the CPL is finished, the DC-link control is activated at $t = 0.2 \text{ s}$. The DC-link voltage follows the reference of 750 V. At $t = 0.4 \text{ s}$, the load is switched
on and consumes 4 kW of active power. Another load step happens at $t = 0.7$ s. In both cases, the DC-link control drives back the DC voltage to the reference value within 200 ms. The islanding inverter reacts to both load changes and quickly restores nominal voltage within at most 40 ms. During the whole operation, the frequency stays close to its nominal value. Thus it can be concluded that the proposed controller design can control both voltage and frequency in an island consisting of nonlinear constant power loads.

The harmonics in the system affect the control stability of the voltage and frequency control loop. Thus, with an increasing share of nonlinear loads, it becomes more and more challenging for the inverter to maintain nominal voltage and frequency values. This can be seen in the increase from 4 kW to 6 kW. In case the CPL gets close to the inverter nominal power, the system might lose controllability.
3.3. Simulation Results

Figure 3.16: Simulation validation with nonlinear constant power load.
3.4 Scalability, Control Stability and Robustness Analysis

In the following, the scalability of the new controller design will be demonstrated. Scalability describes that the proposed design method can be used for small, medium and large nominal power ratings. This is executed in combination with a control stability analysis for each power range and variations of the PWM frequency. The robustness of the controller design is demonstrated by an estimation of the time constant of the current control loop.

3.4.1 Scalability

The analytical expression of the voltage control loop as shown in Figure 3.3 will be investigated in the following. The transfer function $F_{W,V}(s)$ amounts to:

$$
F_{W,V}(s) = \frac{\dot{V}_d}{V_d^*} = \left(\frac{1}{R_{ff}} + \frac{1}{R_L} - \frac{1}{F_{CC}} + \frac{1}{F_{CC}F_{PWM}} + \frac{1}{F_{Li}F_{CF}F_{CC}F_{PWM}} + \frac{F_{Lg} + F_{Li} + \frac{1}{F_{CF}}}{R_L \cdot F_{Lg}F_{Li}F_{CC}F_{PWM}}\right)^{-1} (3.18)
$$

From (3.18) it can be seen, that the composition of the filter components and its design in the frequency domain are crucial for the behaviour and the stability analysis. Further details on the rearrangement of the block diagram in Figure 3.3 can be found in appendix B.

Hence, for the investigation on the stability of the overall voltage control loop, the design procedure of the filter has to be considered, which is a complex and challenging task. In [30], a method is presented which represents the actual state-of-the-art. This method offers a step by step design procedure and explains the important limitations and requirements the designer must consider. Thus, the design parameters that are part of the filter design must be considered in the stability analysis.

The design procedure uses base values for the design of the filter components. These base values ensure that the method can be used irrespective of the inverter’s nominal power $P_n$.

$$
Z_{Base} = \frac{V_{PhPh,RMS}^2}{P_n} \quad (3.19)
$$

$$
I_{Base} = \frac{\dot{V}}{Z_{Base}} \quad (3.20)
$$

$$
C_{Base} = \frac{1}{\omega_n \cdot Z_{Base}} \quad (3.21)
$$

$V_{PhPh,RMS}$ is the line-to-line RMS voltage. In addition, the PWM frequency $f_{PWM}$ and the DC-link voltage $V_{DC}$ are important for the design procedure. Thus it is not enough to check if the overall control is stable for a certain parameter set which only takes into consideration the nominal power. Moreover, the stability needs to be checked for the majority of reasonable combinations and reasonable designs of the whole power electronic generator.

The DC-link voltage is limited in a narrow band. In low-voltage grids, the effective DC-link voltage at the terminals of the Mosfets or IGBTs needs to be at least twice the peak voltage. However, the usage of a transformer will decrease the lower limit of DC-link voltage. But in this case, the impedances and hence the transfer functions of the filter and control loop can again be transformed to nominal grid voltage level. Thus the overall transfer function on the grid level
### 3.4. Scalability, Control Stability and Robustness Analysis

#### Table 3.2: Components of a reasonable LCL filter design, in accordance with [30]

<table>
<thead>
<tr>
<th>$P_n$</th>
<th>1 kW</th>
<th>10 kW</th>
<th>100 kW</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Z_{Base}$</td>
<td>160 $\Omega$</td>
<td>16 $\Omega$</td>
<td>1.6 $\Omega$</td>
</tr>
<tr>
<td>$C_{Base}$</td>
<td>20 $\mu F$</td>
<td>200 $\mu F$</td>
<td>2000 $\mu F$</td>
</tr>
<tr>
<td>$V_{DC}$</td>
<td>750 $V$</td>
<td>750 $V$</td>
<td>750 $V$</td>
</tr>
<tr>
<td>$f_{PWM}$</td>
<td>10 kHz</td>
<td>10 kHz</td>
<td>10 kHz</td>
</tr>
<tr>
<td>$L_i$</td>
<td>30.6 mH</td>
<td>3.06 mH</td>
<td>0.306 mH</td>
</tr>
<tr>
<td>$C_F$</td>
<td>0.497 $\mu F$</td>
<td>4.97 $\mu F$</td>
<td>49.7 $\mu F$</td>
</tr>
<tr>
<td>$L_g$</td>
<td>25 mH</td>
<td>2.5 mH</td>
<td>0.25 mH</td>
</tr>
<tr>
<td>$X_{L,ges}$</td>
<td>11.2 p.u.</td>
<td>11.2 p.u.</td>
<td>11.2 p.u.</td>
</tr>
<tr>
<td>$f_{F, res}$</td>
<td>1.92 kHz</td>
<td>1.92 kHz</td>
<td>1.92 kHz</td>
</tr>
</tbody>
</table>

stays the same, except for nonlinearities of the transformer.

$$V_{DC, \text{min}} > 2 \cdot 230 V \cdot \sqrt{2} \approx 650 V \quad (3.22)$$

The upper limit derives from the used technology for the switches. In simulations and experimental setups, the electrical characteristics demanded a maximum voltage of 750 V. Hence, the variation in DC-link voltage will only have a minor effect on the filter design.

Assuming a fixed PWM frequency results in the filter values that are shown in Table 3.2. With increasing nominal power $P_n$, the inductance values decrease and the capacitance values increase. The design leads to a constant nominated inductive impedance $X_{L,ges}$ in p.u. Furthermore, the resonance frequency stays about one fifth of the switching frequency. Both parameters result from a good filter design, according to [30].

The PWM frequency can vary in distributed generation units. As a rule of thumb, the higher the power, the lower the PWM frequency due to increasing switching losses which limit the PWM frequency. In low-voltage grids, PWM frequencies should remain in the range of 5 kHz to 20 kHz. Hence, the overall stability will be investigated for that frequency range.

#### 3.4.2 Control Stability of the Voltage Control Loop

**Figure 3.17** shows the Nyquist plot for the open loop of different nominal power values and PWM frequencies. The load is set to open circuit conditions. This condition is most critical because in this case there is no damping in the system. Using the simplified Nyquist criterion, it can be seen that all combinations of nominal power and PWM frequency which is set equal to the sample frequency are stable.

**Figure 3.18** shows the Bode plot for a 10 kW inverter with a PWM frequency of 10 kHz. The sampling frequency is equal to the PWM frequency. Both curves show the control behaviour for open circuit conditions. For the black curve (no capacitive load) the stability border of -180° is breached at about 9 kHz. The damping at this frequency is sufficiently high (-30 dB). Assuming a highly capacitive load (grey curve), the stability border is breached at 1.7 kHz, the magnitude is again at -30 dB. Both curves show the overall stability of the voltage control loop for different load conditions according to standard control theory. In appendix C, bode diagrams for other inverter nominal ratings and PWM frequencies are shown.
Chapter 3. Modelling and New Controller Design for Single Inverter Operation

Figure 3.17: Nyquist plot of the open voltage control loop for several nominal power values and PWM frequencies.

Figure 3.18: Bode diagram of the open voltage control loop for a 10 kW inverter under open circuit conditions. Black line: without capacitive load, grey line: with capacitive load equal to nominal capacitance $C_{\text{Base}}$. Even under high capacitive conditions, the control loop is still stable as the phase margin is positive.
3.4.3 Evaluation of the Control Robustness

In control theory, robust controller design addresses the stability analysis in the presence of modelling errors. A robust control loop design is supposed to provide good results despite modelling uncertainties. The major modelling uncertainty of the presented controller design in this thesis is the behaviour of the current control loop. The proposed design procedure of the voltage control loop is based on the assumption that the designer knows the time constant $\tau_i$ of the current control loop. But what if the time constant is unknown? What happens if it needs to be estimated and if there is an estimation error?

Time constants of current control loops are usually selected in the range of 0.5 to 5 ms. A design constraint is the switching frequency of the inverter. The switching frequency should be about 10 times the bandwidth of the closed current control loop [75]. Hence, the current control loop bandwidth can roughly be derived from the switching frequency. Thus it can be concluded that even if the actual bandwidth is unknown, its range is relatively limited. The switching frequency of an inverter should be provided by the manufacturer and often can be found in the documentation. If not, it could be identified using the Fourier transformation and analysing the spectrum.

The design procedure for the voltage control loop chose a relatively high bandwidth ($\tau_V = 4$ ms, bandwidth = 250 Hz) compared to the inner bandwidth of the current controller ($\tau_i = 2$ ms, bandwidth = 500 Hz) in order to show the robustness of the proposed design. If $\tau_i$ is unknown, $\tau_V$ should be designed larger and thus a lower bandwidth of the voltage control loop should be accepted. The larger $\tau_V$, the more the inner and outer control loop are decoupled and thus the voltage control loop becomes more robust. In the following, it will be investigated what the effects are from an overestimation or an underestimation of the inner current control loop.

Figure 3.19 shows the Bode plot of the open voltage control loop for a 10 kW inverter. The voltage control time constant is $\tau_V = 10$ ms. The load is a purely capacitive load which is the worst-case scenario for the stability analysis. Figure 3.20 shows the Nyquist plot. The current control time constant is estimated to be $\tau_{i,\text{guess}} = 2$ ms. The dotted-dashed line shows the control loop behaviour if $\tau_i$ was in fact 0.4 ms which is one fifth of the estimated value and the dotted line shows the control loop behaviour if $\tau_i$ was in fact 10 ms which is five times the estimated value. This is an estimation error factor of five. According to the standard control theory, the control loops are still stable because they have a positive phase margin. However, this positive phase margin becomes smaller if the actual inner time constant is 10 ms. In this case, the inner and outer control loop time constants are the same which is in conflict with a reasonable controller design for cascade control architectures.

To illustrate the effects on the actual voltage behaviour, Figure 3.21 shows the step response for the voltage control loop (open circuit condition, no capacitive load). It can be seen that an overestimation of the current control time constant only has minor effects because the curve for $\tau_i = 0.2$ ms is similar to the curve for $\tau_i = 2$ ms. When $\tau_i = 10$ ms and thus in the range of the voltage control loop, there is a significant coupling. This results in an overshoot of about 15%. But still, the control is stable and shows a good step response.

In summary, the proposed design procedure is also applicable if the time constant of the inner current controller can only be estimated.
Chapter 3. Modelling and New Controller Design for Single Inverter Operation

Figure 3.19: Bode diagram of the open voltage control loop for a purely capacitive load \((C = C_{\text{Base}})\). It is assumed, that \(\tau_{i,\text{guess}} = 2\) ms. Solid line: \(\tau_i = 2\) ms (no estimation error), dotted-dashed line: \(\tau_i = 0.4\) ms, dotted line: \(\tau_i = 10\) ms.

Figure 3.20: Nyquist plot of the open voltage control loop for a purely capacitive load \((C = C_{\text{Base}})\). It is assumed, that \(\tau_{i,\text{guess}} = 2\) ms. Solid line: \(\tau_i = 2\) ms (no estimation error), dotted-dashed line: \(\tau_i = 0.4\) ms, dotted line: \(\tau_i = 10\) ms.
3.4. Simulation Results

In the previous subsection it was shown that the voltage control loop is stable irrespective of the nominal power and in the relevant frequency range. In the following, the step response of the voltage and frequency control is shown in order to compare them. Figure 3.22 shows the step responses for the voltage control loop for different load compositions and different nominal powers of the inverter. It can be seen that the step responses are almost identical for different nominal powers. Thus, the proposed design method is scalable and can be used for various inverters in the low-voltage grid.
Figure 3.22: Simulation results for the scalability of the proposed design method. Step responses of the voltage and frequency control loop for different load compositions and different nominal powers of the inverter.
3.5 Experimental Validation

The experimental setup was composed of an inverter which was connected to a constant DC power supply. Standard LCL filter components were used. Resistive, inductive and capacitive loads were connected to a point of common coupling. The control algorithm was implemented on a dSpace DS 1007 system. For experimental validation of the operation with a CPL, a second inverter with equal filter components and two separate dSpace DS 1007 systems were used to emulate two independent measurement and control systems. Table 3.3 lists the parameters of the experimental tests.

The following experimental results are obtained with $\tau_v = 4 \text{ ms}$. Thus, the voltage control loop is relatively fast compared to the current control loop. This is a challenging condition for the overall control stability.

3.5.1 Linear RLC Loads

For experimental tests with linear loads, the setup of Figure 3.10 is used. The results are presented on pages 57 to 59.

Figure 3.23 shows the experimental results for the step response of the islanding voltage for resistive loads. The grey area represents the theoretical model. The experiment was executed for different active load conditions from zero to nominal power. It can be seen that the experimental tests match the predictions of the theoretical model.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_n$</td>
<td>Nominal power of the inverter</td>
<td>8 kVA</td>
</tr>
<tr>
<td>$V_n$</td>
<td>Nominal RMS grid voltage (line to line)</td>
<td>400 V</td>
</tr>
<tr>
<td>$f_n$</td>
<td>Nominal grid frequency</td>
<td>50 Hz</td>
</tr>
<tr>
<td>$Z_{\text{Base}}$</td>
<td>Base impedance</td>
<td>20 $\Omega$</td>
</tr>
<tr>
<td>$L_iL_g$</td>
<td>Filter inductances</td>
<td>5 / 1.5 mH</td>
</tr>
<tr>
<td>$C_F$</td>
<td>Filter capacitance</td>
<td>5 $\mu F$</td>
</tr>
<tr>
<td>$\tau_i$</td>
<td>Time constant of the current controller</td>
<td>2 ms</td>
</tr>
<tr>
<td>$\tau_V$</td>
<td>Time constant of the voltage controller</td>
<td>4 ms</td>
</tr>
<tr>
<td>$\tau_f$</td>
<td>Time constant of the frequency controller</td>
<td>22 ms</td>
</tr>
<tr>
<td>$R_{\text{ff}}$</td>
<td>Feed-forward impedance of voltage controller</td>
<td>60 $\Omega$</td>
</tr>
<tr>
<td>$K_{P,V}$</td>
<td>Proportional gain of voltage controller</td>
<td>$\frac{1}{60} \Omega$</td>
</tr>
<tr>
<td>$K_{I,V}$</td>
<td>Integral gain of voltage controller</td>
<td>4.167 $\Omega$s$^{-1}$</td>
</tr>
<tr>
<td>$X_{\text{ff}}$</td>
<td>Feed-forward impedance of frequency controller</td>
<td>5 $\Omega$</td>
</tr>
<tr>
<td>$K_{I,f}$</td>
<td>Integral gain of frequency controller</td>
<td>250 As</td>
</tr>
<tr>
<td>$T_s$</td>
<td>Sampling time of the control loops</td>
<td>200 $\mu$s</td>
</tr>
<tr>
<td>$f_{\text{PWM}}$</td>
<td>Switching frequency of the PWM</td>
<td>10 kHz</td>
</tr>
</tbody>
</table>
Chapter 3. Modelling and New Controller Design for Single Inverter Operation

Figure 3.24 shows the step response of the voltage control loop for various resistive-capacitive loads with a constant reactive power demand of $Q_C = 0.25 P_n$. The higher the active power demand, the better the theoretical model fits the experimental results. For a capacitive-only load, there is a small overshoot.

Figure 3.25 shows the step response of the voltage control loop for various resistive-inductive loads with a constant reactive power demand of $Q_{ind} = 0.5 P_n$. It can be seen that damped systems with a realistic quality factor $Q_f \leq 1$ can be controlled as predicted with the theoretical model. The control faces some challenges for inductive-only load conditions. There is a short overshoot and the control variable $V_d$ has some oscillations. This is due to a relatively high amount of harmonics. Thus $V_d$ is not constant because it is superimposed by higher frequencies that are not transformed into constants in the synchronous reference frame. Figure 3.25 also illustrates what happens if the load demand is larger than the inverter's nominal apparent power. The curve for $P_L = P_n$ saturates at a voltage level of 0.9 p.u. This is still a valid islanding voltage. But as the load’s apparent power $S = \sqrt{P^2 + Q^2}$ is larger than the inverter’s nominal apparent power, the current protection and limitation of the inverter only allows a voltage level of 0.9 p.u.

Figure 3.26 shows the disturbance reaction of the frequency control loop for resistive-only loads. The frequency control loop is able to drive the islanding frequency back to nominal value within 0.1 s. The higher the damping of the system, the smaller the initial disturbances.

Figure 3.27 shows the disturbance reaction of the frequency control loop for resistive-capacitive loads with a constant reactive power demand of $Q_C = 0.25 P_n$. Again, the frequency control loop is able to drive the islanding frequency back to nominal value within 0.1 s. In case the reactive power demand is less than $Q_C = 0.25 P_n$, the initial deviations are smaller and frequency can be controlled even more easily. This is not shown here.

Figure 3.28 shows the disturbance reaction of the frequency control loop for resistive-inductive loads with a constant reactive power demand of $Q_{ind} = 0.5 P_n$. Again, the frequency control loop is able to drive the islanding frequency back to nominal value within 0.1 s. In contrast to capacitive and resistive-only loads, the initial frequency deviations are positive. The reason is that in the beginning, the island is lacking positive reactive power demanded by the inductors which leads to increasing frequencies.

Figure 3.29, Figure 3.30 and Figure 3.31 show the behaviour of the reactive voltage component $V_q$ for resistive-only, resistive-capacitive and resistive-inductive loads respectively. $V_q$ is an indicator for the stability and robustness of the frequency control loop in general and in particular for the effectiveness of the feed-forward admittance $X_{ff}^{-1}$. It can be seen that the initial deviations of $V_q$ remain relatively low. The higher the reactive power demand, the higher the deviations. But even for $Q_{ind} = 0.5 P_n$, they remain below 0.15 p.u. In steady-state, the frequency control loop is able to control $V_q$ to zero.

In case, the filter components are not designed carefully, the controllability of voltage and frequency might suffer. Then, resonance frequencies of the filter and the load might get close to the switching frequency or the current controller bandwidth. If this is the case, the $dq$ variables get superimposed with oscillations due to an increase in harmonics. In addition, it becomes more and more challenging to remain a stable control of voltage and frequency for open circuit conditions. In appendix D, experimental results for an LC filter and a transformer setup can be found. The LC component design was intentionally sub-optimal to highlight the effects. Thus the controllability suffers especially for poorly damped conditions. In summary, it can be stated that the more carefully the filter and current control loop are designed, the better the control stability for the voltage and frequency control loop.
3.5. Experimental Validation

Figure 3.23: Experimental results for the step response of the voltage control loop for resistive load conditions. Model is marked by grey area. $\tau_v = 4$ ms.

Figure 3.24: Experimental results for the step response of voltage control loop for resistive-capacitive load conditions. Model is marked by grey area. $\tau_v = 4$ ms.

Figure 3.25: Experimental results for the step response of voltage control loop for resistive-inductive load conditions. Model is marked by grey area. $\tau_v = 4$ ms.
Chapter 3. Modelling and New Controller Design for Single Inverter Operation

Figure 3.26: Experimental results for the disturbance reaction of frequency control loop for resistive load conditions. $\tau_l \approx 20$ ms.

Figure 3.27: Experimental results for the disturbance reaction of the frequency control loop for resistive-capacitive load conditions. $\tau_l \approx 20$ ms.

Figure 3.28: Experimental results for the disturbance reaction of the frequency control loop for resistive-inductive load conditions. $\tau_l \approx 20$ ms.
3.5. Experimental Validation

Figure 3.29: Experimental results for the disturbance reaction of the reactive voltage component \( V_q \) for resistive load conditions. \( X_f = \frac{1}{4} Z_{\text{base}} \).

Figure 3.30: Experimental results for the disturbance reaction of the reactive voltage component \( V_q \) for resistive-capacitive load conditions. \( X_f = \frac{1}{4} Z_{\text{base}} \).

Figure 3.31: Experimental results for the disturbance reaction of the reactive voltage component \( V_q \) for resistive-inductive load conditions. \( X_f = \frac{1}{4} Z_{\text{base}} \).
3.5.2 Constant Power Loads

For the experimental tests with the constant power load (CPL), the setup of Figure 3.15 is used. The CPL is designed using a controlled rectifier with a resistive load on the DC-side. The filter and current control values are equal to the generator side (see Table 3.3). Due to equal time constants, the robustness of the applied controls can be tested appropriately. The DC-link time constant was designed to be about 100 ms. In order to represent a mixture between linear and nonlinear loads in low-voltage grids, a resistor was put in parallel to the CPL. The active power consumption of the CPL is about 1 kW, the resistive load power consumption is about 2 kW.

The results are shown in Figure 3.32. The inverter establishes the nominal voltage within 0.1 s. The load is activated but non-controlled during the first 5 s which is the wake-up time of the inverter. At \( t = 5 \) s, the DC-link control is activated and a constant power is consumed. After 2 s, the nominal active power consumption is changed to a lower value and after another 2 s, another step of the load is performed.

Figure 3.32 (a) and (b) show voltage and frequency respectively. During the whole operation (non-controlled, controlled and power steps), the nominal values can be maintained and disturbances are rejected quickly. Figure 3.32 (c) shows the active power demand of the load. Due to the relatively high share of harmonics in the system, the instantaneous power (grey curve) is not very useful and thus it is filtered with a low-pass-filter (black curve) to show the step in power consumption. This experiment verifies that the proposed control is able to supply nonlinear constant power loads.

The experiment is repeated without the linear 2 kW load, as shown in Figure 3.33. Without the linear load it is even more challenging for the inverter to control voltage and frequency to nominal values because there is no damping in the system. The test procedure is analogue to the previous test. Because there is no damping, the instantaneous values for voltage and active power demand contain more harmonics. But still the control is stable and the CPL can be supplied.

The system might become unstable if the CPL is further increased. It is unlikely that a CPL which has a power demand close to the nominal power of the inverter can be supplied successfully without any damping in the system. Maybe, improved current control strategies incorporating active harmonic damping or similar approaches might be more suitable for this test case. Today, it might be better not to assume that the majority of existing inverters in the grid is equipped with very robust current control loops. However, the potential of increased current control robustness is in the focus of research. In the future, this could be an interesting approach to investigate the effects of highly skilled current control loops on the controllability of CPL in poorly damped islanded grids. In this case, the ordinary state-of-the-art current controller that was used in this thesis could be substituted.
3.5. Experimental Validation

Figure 3.32: Experimental results for operation with a composition of a linear load (2 kW) and a constant power load (1 kW), implemented with a controlled rectifier. (a) voltage, (b) frequency, (c) active power. The grey data are instantaneous values. They have a high share of harmonics due to harmonics in islanding voltage and currents. For the filtered data, a low-pass filter with a time constant of 5 ms was used.
Figure 3.33: Experimental results for operation with a constant power load only (1 kW). The grey data are instantaneous values. They have a high share of harmonics due to harmonics in islanding voltage and currents. For the filtered data, a low-pass filter with a time constant of 5 ms was used.
Chapter 4

Novel Multiple Inverter Control Strategy

In the previous chapter a new design method for the voltage and frequency control of three-phase inverters for islanding operation was developed. The next step is the development of a control strategy that can be used in both single and multiple inverter islands. A start-up procedure from zero-voltage conditions including a novel cooperative voltage and frequency control is presented which does not need communication. Non-controllable generation (NCG) is integrated into the control strategy and effective countermeasures against an excess of active power are demonstrated. Experimental tests in the laboratory confirm the effectiveness of the novel control strategy and illustrate its benefits.

4.1 Requirements on Multiple Inverter Operation

Figure 4.1 illustrates an example for a simplified single line equivalent circuit of a possible low-voltage grid containing several loads and generation units. One has to distinguish between controllable and non-controllable generation (NCG). Controllable generation incorporates the voltage and frequency control loops that have been designed in chapter 3. They are part of the multiple inverter control strategy that is proposed in the following. NCG is not part of the control. These are e.g. ordinary PV plants—grid feeding units without voltage and frequency controllers. The voltage and frequency control for the setup of Figure 4.1 must be able to maintain nominal values of voltage and frequency for single and multiple inverter generation.

Figure 4.1: Simplified single-phase equivalent circuit for multiple inverter islanding operation. Several loads and controllable (M/F) or non-controllable (NCG) inverters are connected.
This should be possible without communication because of the large number of generators in low-voltage grids and the high costs that would be imposed by additional communication links.

There are two main approaches for the operation of multiple inverters in parallel. The first approach is active load sharing, where information is shared among inverters via communication. Only a single voltage source (grid forming unit) and several current sources (grid feeding units) are used. There are two mechanisms for this approach: 1) the average current/power sharing scheme and 2) the master-slave sharing scheme.

The average current/power sharing scheme is proposed in [82] and [83]. All inverters participate in both voltage and current control. Therefore a communication link for the reference values is used. This approach achieves good results for power sharing and voltage quality. But if communication fails among the generation units, the system is not able to operate. Furthermore, it is challenging to include external generation units that have not been adapted to the active power sharing scheme.

The master-slave sharing scheme is described in [43, 84, 85]. The master operates as a voltage source and multiple slaves act as current sources. The share of each generation depends on the output impedance. Again, information for load sharing is spread via a communication link. Master-slave sharing methods have some drawbacks in common. The grid forming unit must be able to initially increase the grid voltage to nominal values without the support of other inverters. Furthermore the whole system is not stable if the grid forming unit has an outage and none of the slaves is able to take the master’s role [38]. And—most critically—like all current/power sharing schemes, this concept requires communication.

In summary, the challenging inclusion of additional generators, the vulnerability to master outages and the dependence on communication disqualify the current/power sharing scheme as a possible control strategy for the problem that is discussed here.

The second approach is to operate with multiple voltage sources. In this case, an adequate and proper power sharing among the voltage sources must be implemented. Most commonly, the droop control is used to share active and reactive power between the voltage sources [33]. But fluctuations in loads and generations lead to small deviations from the set-point. This is also dependent on line impedances [86]. This can be corrected with the help of a hierarchical control structure [87]. A secondary controller (centralised or decentralised) is required to eliminate steady-state errors by providing reference values for each generation unit. But this requires communication infrastructure [36–39].

The droop control approach seems to be more suitable for islanding operation than the current/power sharing scheme. This is the reason why it is used in many microgrid control structures. However, the necessity of a secondary controller level and the dependence on communication impede the usage of this concept because it would result in steady-state errors. Besides, unknown load conditions make it relatively challenging to choose suitable set-points for active and reactive power. These disadvantages can be taken care of in carefully designed microgrid structures. But this might not be suitable for the large number of diverse low-voltage grids with volatile generation and load conditions.

In the following, a novel cooperative voltage and frequency control concept is proposed that combines the advantages of the droop control and the advantages of the master-slave concept. The development of this novel control concept can be split into two steps which provide answers to the following questions: How to define which inverter takes which role in the island (section 4.2)? And what are the effects of the role assignment for the individual inverter (section 4.3)?
4.2 Procedure from Zero-Voltage Conditions and Overall Control Concept

In the following it will be assumed that the disconnection device of Figure 4.1 disconnected the low-voltage grid from the rest of the utility grid. In this case, the voltage will eventually be zero because the generation units will detect islanding and trip if they are equipped with anti-islanding detection as stipulated in the grid codes. The spatial extent of low-voltage grids is relatively small [16–19]. Thus—neglecting line impedances—it can further be assumed that the voltage level is similar in the whole low-voltage island. Besides, it is assumed that there is no residual voltage in the grid. This is the initial condition for the novel procedure which is described in the following.

First, it needs to be determined, which of the controllable inverters takes the lead in the island. It is defined as the Master inverter. The other inverters will be defined as so-called Followers. As the composition of generation units is unknown and could change from time to time, an adaptable but deterministic process is needed.

The Master unit will have the main responsibility for voltage and frequency stabilization in the islanded grid. Thus it is obvious to choose the largest inverter to become the Master. There are two possibilities to define an inverter as the largest: its nominal power ratings and its actual power at the moment of the islanding operation. Although the actual power seems to be most important for islanding operation, it is wise to choose the Master with the highest power ratings due to the following reasons:

- For frequency control, reactive power is required. The Master with the highest nominal power is able to provide the highest amount of reactive power irrespective of the actual active power that is available. Thus it is possible to provide islanding operation for a wider range of reactive power demand. In addition, the provision of reactive power is also important to influence the behaviour of non-controllable generation.

- The operation of small low-voltage islands might be the first step of a whole power system restoration in the case of a wide-area blackout. In the future it might be useful to equip a small group of large generation units with an additional communication unit in order to coordinate a restoration process of the whole distribution grid. In this case it is more reasonable to have the Master unit equipped with the communication unit. Nominal power ratings could be better known than the actual power right before a blackout event. Hence the transformation of the whole system can be planned more easily and step by step by choosing those generation units which have a high power rating. Although a solution of such a complex problem goes beyond the scope of this thesis, the mentioned considerations should be kept in mind because they could be of relevance for future research.

Figure 4.2 shows the process for discrimination between Master and Follower. It is initiated when voltage collapses and is initially close to zero. After the voltage collapse, all possible Masters or Followers (M/F) wait for a specific amount of recreation time $t_{rec}$ which depends on the respective nominal power $P_n$.

$$
t_{rec} = t_{safe} + t_{flex} + t_{rand} = t_{safe} + \frac{c}{P_n} + t_{rand} \quad (4.1)
$$

The recreation time is composed of a safety margin $t_{safe}$, an inverter dependent time $t_{flex}$ and an additional small random time $t_{rand}$. The safety margin is constant for all inverters and can be used to maintain zero-voltage for at least a specific amount of time. $t_{flex}$ depends on the inverse
of the inverter power ratings and a design constant \( c \) \( ([c] = s \cdot W) \). This means, the higher the nominal power of an inverter, the smaller \( t_{\text{flex}} \).

For example, if \( c \) was set to \( c = 20 \text{ s} \cdot \text{kW} \), a 10 kW inverter would try to start islanding after 2 s, a 5 kW inverter after 4 s, etc. In order to prevent two inverters with the same nominal power starting at the same time, a small random time constant \( t_{\text{rand}} \) is added to \( t_{\text{rec}} \). Properly speaking, by adding a random time constant, the procedure is no longer deterministic. But if \( t_{\text{rand}} \) is chosen within a reasonably small time interval, it only has an effect if there are multiple inverters with the same nominal power ratings. However, the interval must not be too small in order not to be in the range of the inverter sampling time. The sampling time usually is in the range of several hundred microseconds. Of course, the usage of a random time constant is stretched to its limits if the number of equally sized inverters is relatively high which could be the case for very large low-voltage grid structures. On the other hand, very large low-voltage grid structures might be a good field of application for specially designed microgrids including hierarchical control structures.

If the voltage is still zero after \( t_{\text{rec}} \), the inverter becomes a Master. If grid voltage is not zero when \( t_{\text{rec}} \) expired, the inverter becomes a Follower. Let there be two inverters A and B in the island. While inverter A is waiting for \( t_{\text{rec}} \), two scenarios are possible.

- The voltage is still zero after \( t_{\text{rec},A} \). In this case, inverter A can determine that it is the largest inverter in the island because if there was a larger one, it would already have tried

Figure 4.2: Flow chart for procedure from zero-voltage condition. Left: controllable inverters (Master/Follower), right: non-controllable inverters (NCG).
to increase voltage. Thus inverter A becomes the Master.

- The voltage has already been increased fully or partly by inverter B whilst waiting for \( t_{\text{rec,A}} \). In this case, inverter A knows that inverter B already declared itself the Master because it has a higher power rating than inverter A. Thus inverter A becomes a Follower.

As soon as the first inverter becomes a Master, it tries to start islanding immediately. Thus, the other inverters become Followers immediately—even before their \( t_{\text{rec}} \) has expired except for a small time delay for measuring and computing the grid voltage.

When the Master activates its control and tries to energise the island, its amount of active power might not be sufficient. Followers will join after \( t_{\text{delay}} \). Thus they can support the Master with their active power and cooperatively restore grid voltage. \( t_{\text{delay}} \) needs to be chosen with respect to the time constant of the voltage control loop. As designed in chapter 3, the voltage control loop of an inverter is able to reach its maximum output power within less than 20 ms. Thus, \( t_{\text{delay}} \) is defined 100 ms.

During the start-up phase, anti-islanding detection (AID) needs to be deactivated because obviously it will take some time until the voltage is inside the voltage limits. After all generators joined, voltage and frequency must remain inside the limits and AID can be turned on. But only voltage and frequency monitoring may be activated. Of course, active AID methods such as slip mode frequency shifting must remain deactivated because they could destabilise the island. This is the case if the amount of active and reactive power is sufficient. If the total provision of the active power of Master and Followers is not enough to bring voltage above the minimum limit of \( V_{\text{min}} = 80\% \, V_n \) within \( t_{\text{M,F}} = 200 \, \text{ms} \) from the moment the Master started, the inverters can detect this and shut-down operation. If voltage is above \( V_{\text{max}} \), inverters will shut-down as well. The same applies to frequency. The task of validating voltage and frequency limits can actually be reduced to the simple check for under voltage. The reason for this is that the control method of each inverter is defined to give reactive current preference over active current. This means that frequency control has a higher priority than voltage control. Thus, if the inverter reaches its ampacity limit, its active power will be reduced first which leads to a reduction of the voltage whereas the frequency can still be controlled at nominal value. From this it can be derived that as long as the voltage is inside the allowed range, the frequency can definitely be controlled at its desired value. This holds true even in the unlikely event that the loads demand more reactive power than active power.

With the proposed schedule, the possibility of collecting enough power for operation of the island can be maximised. No additional communication is needed as the inverters indirectly communicate via the voltage. With this, every inverter can effectively discriminate its role in the island and the islanded grid can be operated conjointly. The novel method is both deterministic and adaptable. It is deterministic because due to the recreation time, the result is predictable except for the small random time which becomes effective if there are multiple inverters with the same nominal power rating. It is adaptable because it can be used for diverse combinations of nominal power ratings.
4.3 Novel Cooperative Voltage and Frequency Control

4.3.1 Problem Description

Figure 4.3 shows a simplified diagram of the controllers that have been developed in chapter 3. Both voltage and frequency controller consist of a proportional and an integral term. In the voltage control loop, there are two proportional terms: $K_{P,V}$ of the PI controller and the feed-forward admittance $R_{ff}^{-1}$. The integral term is the integral term of the PI controller. In the frequency control loop, the feed-forward admittance $X_{ff}^{-1}$ represents the proportional term and the integral term comes from the frequency I controller.

When there are multiple inverters that try to control the islanding voltage and frequency at exactly nominal value by using an integral term to drive the steady-state error to zero, circulating currents might occur [40]. Due to non-ideal offsets in the measurement or control of each inverter, it could happen that two inverters have two different set-points and work against each other. Much worse, control instabilities might occur. Thus, special attention should be paid to carefully design multiple control integral terms inside a single system.

Let both inverters A and B have a set-point of 50 Hz for frequency control. But due to a measurement error, inverter B has an offset of $\Delta f = -10$ mHz, thus always sees a frequency that is below the reference value of 50 Hz. The integral term in both controllers would make inverter B provide more and more reactive power. Inverter A would always try to reduce the overall reactive power. Thus, the (integral) controls work against each other.

![Figure 4.3: Novel cooperative voltage (a) and frequency (b) control strategy for Master and Follower inverters: Both controllers consist of proportional (dashed line, $K_{P,V}, R_{ff}^{-1}, X_{ff}^{-1}$) and integral controller parts (dotted line, $K_{I,V}, K_{I,f}$). The plant represents the current controller and the load.](image-url)
Because of this, in electrical power systems, the control algorithms in the respective power plants only use proportional terms (droop), for example the primary frequency control. If there is only a proportional term, there will always be deviations of the nominal value. Hence a central secondary controller changes the respective reference values for every generator to restore nominal values. There is only one central controller in a regulation zone which has an integral term and thus no two controllers can work against each other.

This concept works for the whole electrical power system and has been introduced in microgrids as well. The standard hierarchical control concept for microgrids consists of droop controllers at every generation unit. This represents the proportional term, hence primary control. Secondary control is implemented in a central secondary controller that has the same function as in bigger power systems. It provides the respective reference values for the generators and thus reduces deviations from nominal values to zero [87].

Using this concept here is not suitable due to several reasons. It cannot be taken for granted that there is a communication link that provides reference values for each generation unit. In fact, a control strategy is required which is independent of communication and still is able to operate without a steady-state error. Besides, it is not clear, how many generation units there are in an island. This demands for a control strategy which is working irrespective of the number of generation units. The proposed cooperative voltage and frequency control of this thesis uses a dead-band concept which is presented in the following.

### 4.3.2 New Control Approach

When operating in low-voltage islanding systems, a control strategy is required that is independent of a communication structure. Nevertheless it must be able to control voltage and frequency to nominal values. If only a droop control is implemented but the central secondary control is missing, this would result in steady state deviations. Instead the Master / Follower concept of the previous section is used to design a proper overall control strategy.

The Master always operates with both proportional and integral controller term. Thus as long as its power reserve is sufficient, the Master will drive the steady-state error to zero and maintain nominal values. Followers use a different concept, which is shown in Figure 4.4. Both the voltage and frequency control incorporate a dead-band. As long as the actual values remain

![Figure 4.4: Concept of dead-band control of voltage and frequency that is implemented in Followers. In contrast to the Master, the Followers only activate their integral control part, when the control error exceeds certain limits $\pm \Delta$. Inside the dead-band, only proportional control is active.](image-url)
inside the dead-band, the Followers only use their proportional term of the controller. Thus in this area only the Master has an active integral term that drives the steady state error to zero. If actual values deviate too much and exceed the dead-band limits, the Followers activate the integral term of their controller. This supports the Master as the Followers can help to drive back voltage or frequency to nominal values. After nominal values are reached, the Followers deactivate their integral term. The integral terms of the Master and the Followers do not work against each other. If the voltage is too high, all inverters measure a positive deviation and reduce their active power. Thus, all inverters control the voltage to the same direction towards the nominal value. Control instabilities could occur when multiple integral controllers remain activated from the moment when the nominal value is reached. But then, the Followers deactivate their integral term and only the proportional term is active.

With this control concept, every generator can be equipped with its own secondary controller but interferences between the controllers are avoided. Because of this, no deviations can occur that are greater than the dead-band. The dead-band is violated as soon as the Master cannot provide enough active or reactive power. This activates the Followers which can support to drive back the error to zero. Furthermore this concept uses the full potential of each Master and Follower. If there is a backup of active or reactive power, it can be used as soon as the loads demand for it. Even if the Master would be over-challenged, all Followers support the stabilisation of voltage and frequency.

The proposed control combines the benefits of the droop control without its drawback of steady-state errors. A proportional term only is similar to a droop curve. The activation of the integral term of each inverter causes a shifting of the droop curve in a way that the nominal voltage and frequency values are reached eventually.

The proposed method also has some disadvantages. It is not able to ensure a certain power sharing between several generation units. The violation of the dead-band mainly results from the power limitation of the Master. Thus, the Master operates without a power reserve. Besides, when multiple Followers are activated due to a dead-band violation, the additional active/reactive power results from the respective integral controller parameters. If the integral term is designed in accordance with the design procedure of chapter 3, it depends on the inverter nominal power. There might be cases in which another power sharing might be more suitable. The droop control method is able to define a power sharing by providing reference values via the secondary controller and a communication link. But as the proposed control method of this thesis does not incorporate communication, no reference values are provided.

4.3.3 Additional Benefits

Normally the Master concept faces the drawback that the controlled system is likely to collapse in case the Master fails. But with the proposed control strategy, the Followers are still able to handle a Master outage and stabilise the system because as soon as the actual voltage or frequency violates the dead-band limits, Followers drive back the system to nominal value.

Furthermore, this concept of distributed cooperative control could give an answer to large voltage deviations in mainly resistive low-voltage grids. Low-voltage grids have a high $R/X$ ratio. Thus if there are large loads, local voltage drops because of the high currents. If the proposed control concept is used, the Follower which is closest to the large load measures the under-voltage. As soon as the voltage drops below the dead-band, the inverter increases its active power and drives the voltage back to nominal value. This is especially useful for relatively big low-voltage islands with long cables and concentrated load demand like in industrial areas.
4.3. Novel Cooperative Voltage and Frequency Control

Figure 4.5: Example for automatic voltage balancing when using the proposed dead-band control strategy. (a) voltage level if only the Master supplies the loads, (b) voltage level if the Follower supports the local load.

Figure 4.5 (a) shows an example of a simplified voltage curve in an islanded grid. The farther away from the Master, the lower the voltage. If voltage eventually drops below the lower dead-band limit, the Follower activates its integral term and drives back voltage to nominal value as shown in Figure 4.5 (b).

4.3.4 Simulation Results

Figure 4.6 shows the simulation setup for a multiple inverter operation with three controllable inverters with nominal powers of 10 kW, 7.5 kW and 5 kW. The loads L1 and L2 are connected at the ends of the island. The line impedance is modelled as a resistive-inductive impedance of a NAYY 4x70 cable, which is a relatively small low-voltage cable with a diameter of 70 mm² [20]. It amounts to \( R' \approx 0.5 \, \Omega/km \) and \( X' \approx 0.08 \, \Omega/km \) [21]. The cable length will be varied in simulations to illustrate the controller behaviour when they are electrically close or far away from each other.

Figure 4.6: Simulation setup for multiple inverter operation with three controllable inverters: nominal powers of 10 kW, 7.5 kW and 5 kW. Line impedance of a NAYY 4x70 cable.
Table 4.1: Parameters for simulation of procedure from zero-voltage condition and load adaptation.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{n1,M}$</td>
<td>Nominal power of the Master</td>
<td>10 kW</td>
</tr>
<tr>
<td>$P_{n2,F1}$</td>
<td>Nominal power of the Follower 1</td>
<td>7.5 kW</td>
</tr>
<tr>
<td>$P_{n3,F2}$</td>
<td>Nominal power of the Follower 2</td>
<td>5 kW</td>
</tr>
<tr>
<td>$P_M$</td>
<td>Active power of the Master</td>
<td>1 kW</td>
</tr>
<tr>
<td>$P_{F1}$</td>
<td>Active power of the Follower 1</td>
<td>4.5 kW</td>
</tr>
<tr>
<td>$P_{F2}$</td>
<td>Active power of the Follower 2</td>
<td>4.5 kW</td>
</tr>
<tr>
<td>$P_L$</td>
<td>Active power of the load, equally shared between L1 and L2</td>
<td>$10 \mid 5 \mid 10$ kW</td>
</tr>
<tr>
<td>$Q_L$</td>
<td>Reactive power of the load, equally shared between L1 and L2</td>
<td>$5 \mid 2.5 \mid 5$ kW</td>
</tr>
<tr>
<td>$l_{cable}$</td>
<td>Cable length</td>
<td>0 m</td>
</tr>
</tbody>
</table>

Zero-voltage procedure and adaptation to load steps

Figure 4.7 shows the simulation results for a setup with three inverters of different nominal powers and actual power as listed in Table 4.1. The length of the cables is set to zero to investigate the behaviour of multiple inverters at a single point of common coupling. Besides, the Master unit only provides 10% of the actual active power although it has the highest power rating. This can be the case if the number of inverter-based generation in a single island is relatively large and the Master’s share is small.

At $t = 0$ s, the largest inverter determines itself as the Master and starts energising the island. This tells the other inverters that they are Followers. The Master’s actual power is below the load demand and initially only a voltage level of about 30% is reached, as shown in Figure 4.7 (a). The voltage saturates at $V \approx \sqrt{\frac{1000}{10000}} \cdot V_n = 0.32$ p.u. After the delay time $t_{\text{delay}} = 0.1$ s, the Followers F1 and F2 join and support the Master by providing the lacking amount of active power. Conjointly, nominal voltage is reached within 200 ms and the Followers disable their integral control term. At $t = 0.4$ s, 50% of the load is disconnected. This leads to an overshoot in voltage which is controlled back to nominal value within the fundamental period as can be seen in Figure 4.7 (e). The frequency disturbance rejection drives the frequency back to nominal value within 200 ms, as shown in Figure 4.7 (d). Both voltage and frequency control is accomplished by the adaptation of active and reactive power of three inverters which is shown in Figure 4.7 (c). The Master changes the reactive power, the Followers reduce their active power. At $t = 0.8$ s, the load is set back to its initial value. Again, the voltage and frequency transients are controlled within 20 ms and 200 ms respectively.

The simulation illustrates the potential of the novel control strategy. Although the Master only has a low share of the total active power, the voltage can be controlled to nominal value within 200 ms. Relatively large load steps can be controlled. Multiple inverters can be connected to the same point of common coupling without mutual disturbance.
4.3. Novel Cooperative Voltage and Frequency Control

Figure 4.7: Simulation for the procedure from zero-voltage condition and load adaptation, using a Master and two Followers: (a) voltage, (b) activation signals for Master and Followers, (c) power provided by Master $P_M, Q_M$ and Followers $P_{F1,F2}, Q_{F1,F2}$, (d) frequency, (e) transient voltage during load step.
Table 4.2: Parameters for simulation of voltage balancing and line impedances.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{n1,M}$</td>
<td>Nominal power of the Master</td>
<td>10 kW</td>
</tr>
<tr>
<td>$P_{n3,F2}$</td>
<td>Nominal power of the Follower 2</td>
<td>5 kW</td>
</tr>
<tr>
<td>$P_M$</td>
<td>Active power of the Master</td>
<td>10 kW</td>
</tr>
<tr>
<td>$P_{F2}$</td>
<td>Active power of the Follower 2</td>
<td>4 kW</td>
</tr>
<tr>
<td>$P_L$</td>
<td>Active power of the load L2</td>
<td>5 kW</td>
</tr>
<tr>
<td>$l_{\text{cable}}$</td>
<td>Cable length</td>
<td>2 km</td>
</tr>
<tr>
<td>$\Delta V$</td>
<td>Voltage deviation when the integral control is activated</td>
<td>0.05 $V_0$</td>
</tr>
</tbody>
</table>

Voltage balancing with distributed inverters and line impedances

For the simulation of the voltage balancing, the setup of Figure 4.6 is changed. Inverter 2 and load L1 are not used. The cable length is set to 2 km each, thus the total cable length between the Master and the load is 4 km which is relatively unrealistic, especially for a 70 mm² cable. This allows to investigate the controller behaviour in case they are electrically far from each other. Besides, there is a significant voltage drop on the line. Additional parameters can be found in Table 4.2.

Figure 4.8 shows the results for the simulation. First, the Master reaches nominal voltage at its point of common coupling. Due to the voltage drop on the cable, the voltage level at the load is lower. After the Follower joins, it activates its integral term of the voltage controller when the voltage dead-band is violated. This is shown in Figure 4.8 (b). Due to fluctuations and noise in the system, this happens several times as can be seen in Figure 4.8 (a). This leads to an increase of the Follower’s active power and a reduction of the Master’s active power as shown in Figure 4.8 (c). With this, over time the voltage level at the load comes closer to nominal value. After $t = 1.1$ s, no more violations of the dead-band occur and the Follower only operates with its voltage controller proportional term. The short window period when both the Master’s and the Follower’s integral terms are active, do not lead to control instability. In addition, the two voltage controllers do not disturb each other over a long electrical distance. However, in this special case, the steady-state error at the terminals of the load L2 cannot be reduced to zero with the Master. This is due to the large cable impedance of 2 km and due to the relatively large dead-band that has been chosen to illustrate the general principle. Normally, the dead-band could be set closer to the nominal value. But still, the Master maintains nominal value at its terminals.
4.3. Novel Cooperative Voltage and Frequency Control

Figure 4.8: Simulation results for the voltage balancing due to relatively large line impedances. The terminal voltage low-pass filter time constant in (a) is 20 ms.
4.4 Countermeasures against an Excess of Active Power

4.4.1 Problem Description and Background

If there is too much active power in the island, the upper voltage limit will eventually be exceeded. When this happens, all generators will disconnect from the grid immediately. This variation in active power can lead to a collapse of the island. Master and Follower units are not the problem because they control their output power dependent on the islanding voltage. But non-controllable generation (NCG) is the core of the problem. An excess of active power in an islanded grid can either occur when the load remains constant and the NCG increases or if the NCG generation remains constant and the load demand decreases.

Generators connected to the low-voltage grid must provide ancillary services [52]. One of these services is the reduction of active power due to over-frequency, also called \( P(f) \) control. In the past, photovoltaic (PV) inverters had to disconnect from the grid when frequency exceeded 50.2 Hz [51,88]. As the amount of installed PV inverters increased, this method rose the problem that in case of a frequency event in the European grid, all the installed PV generation would trip at the same time and thus leading to a major hazard for the system stability. The solution for this problem was to stipulate a curve that would decrease active power not at once but gradually.

Today, generators must provide a curve which is shown in Figure 4.9 by a black solid line. Their actual active power output \( P_{\text{act}} \) is a function of the system frequency \( f \).

\[
P_{\text{act}} = \begin{cases} 
0 & \text{for } f < 47.5 \text{ Hz} \\
1 & \text{for } 47.5 \text{ Hz} \leq f \leq 50.2 \text{ Hz} \\
P_0 \cdot \left(1 - \frac{0.4}{50.2} \cdot (f - 50.2 \text{ Hz})\right) & \text{for } 50.2 \text{ Hz} < f \leq 51.5 \text{ Hz} \\
0 & \text{for } f > 51.5 \text{ Hz}
\end{cases}
\]  

(4.2)

\( P_0 \) is the active power that was provided just before the frequency exceeded 50.2 Hz.

Grid codes stipulate, that generators must not increase their power any further when the system frequency exceeds 50.2 Hz [52]. In fact, they have to stay on the curve of Figure 4.9 until the

![Figure 4.9: Comparison between the active power reduction due to over-frequency as prescribed in the grid codes and the Frequency-Shift Power control (FSPC) of the inverter manufacturer SMA.](image)
frequency normalises to below 50 Hz for at least 60 seconds [52]. This mandatory behaviour will be used for the novel indirect control which is proposed in this thesis.

4.4.2 Existing Solution and its Limitations

The inverter manufacturer SMA implemented the so-called Frequency-Shift Power Control into its Sunny Boy Backup systems [89]. The SMA inverters are connected to a battery storage system. In case the battery storage system is fully charged and the available power of the primary energy source (solar radiation) exceeds the load power demand, the inverter recognises this situation and increases the frequency of the AC output. As soon as the frequency exceeds a certain value, SMA inverters reduce their active power as shown in Figure 4.9 (dashed line). This system was designed specifically for islanding backup systems of SMA and it is not compatible with other generation units. Besides, it requires the existence and the monitoring of a battery storage system in the island. Thus, this concept cannot be transferred to normal islanding operation because its usability is limited to Sunny Backup systems and is not suitable for any other inverter-based generation.

Hence, a new concept is developed here which can be used by a large number of inverters irrespective of the manufacturer and the implemented control concept. First, the controlling inverter (Master) does not use a battery voltage but the islanding grid voltage for the activation of the new control. Second, the frequency changes the Master is imposing can be interpreted by any generation unit which provides the \( P(f) \) control in accordance with the grid codes. This can be ensured by using the active power reduction curve of Figure 4.9 (black solid line), because this curve is mandatory to all generation units.

4.4.3 New Solution

The proposed control strategy is shown in the flow chart of Figure 4.10. In case there is an excess of active power in the island, the voltage will increase. As soon as it exceeds a certain limit \( V_{\text{lim}} \), the Master changes islanding frequency above 50.2 Hz. Thus NCGs reduce their active power as shown in Figure 4.10 (a); and/or stop the increase of active power as shown in Figure 4.10 (b). Thus the increase in voltage is stopped. For this control, the RMS voltage is used because the actual voltage might have some transients. The RMS value provides low-pass-filter behaviour and is thus more suitable for this control.

Followers must be able to discriminate between an intentional rise of frequency in order to reduce the power of NCG and an unintentional rise of frequency due to a lack of reactive power. The discrimination is not a problem for Followers because there is a significant difference between the two cases. An intentional increase of frequency is only initiated if the islanding voltage is above the limit \( V_{\text{lim}} \) and if the Follower’s active power is zero. Otherwise the Follower would reduce its active power which would decrease the islanding voltage. Thus, as long as the actual voltage is below this limit, the Follower can operate as usual. If the actual voltage is above the limit \( V_{\text{lim}} \), the Follower blocks its integral term. Then the Master is able to increase the frequency by providing reactive power without the Followers providing the inverse reactive power. In the following, the potential of the method will be calculated.
Chapter 4. Novel Multiple Inverter Control Strategy

islanding operation

excess of active power?

no

normal islanding operation

yes

increase in islanding voltage \( V_i \)

\( V_i > V_{lim} \)

no

yes

Master increases frequency above 50.2 Hz

(a)

power reduction (40% per Hz)

no increase of active power

(b)

increase in voltage \( V_i \) is stopped

Figure 4.10: Flow chart for the activation of frequency dependent active power reduction in NCG units. Active power is reduced (a) and/or a further increase of active power is stopped (b).

Decrease of Load Demand

Equation (4.2) shows that it is possible to use the system frequency to control the NCG output active power. The potential of this method can be calculated from the voltage limits for low-voltage grids, which is from 80% to 110% of nominal voltage. For the power demand \( P_L \) of linear RLC loads, the minimum and maximum value for active power provision \( P_{NCG} \) can be calculated:

\[
P_{NCG,\text{min}} = \frac{0.80 \cdot V_n}{R} \leq \frac{V_i^2}{R} = P_L \leq \frac{1.10^2 \cdot V_n^2}{R} = P_{NCG,\text{max}} (4.3)
\]

\( P_L \) is the nominal load demand at nominal voltage \( V_n \). Thus, if NCGs provide more than \( P_{NCG,\text{max}} = 1.21 \cdot P_L \), the over-voltage limit is violated. If all NCGs decrease their active power by 40% per Hz when the frequency exceeds 50.2 Hz, \( P_{NCG,\text{max}} \) extends to:

\[
P_{NCG,\text{max,ext}} = \frac{1.21 \cdot P_L}{1 - \frac{0.4}{51.5 - 50.2}} = 2.52 \cdot P_L (4.4)
\]

Equation (4.4) shows that the actual NCG power can be increased up to 2.52 \( P_L \). In other words, the load demand could be 40% of the initial NCG active power.

If islanding voltage and frequency are changed, both the load and NCGs will have different active power consumption and generation. The index 0 indicates the active power at nominal values. The reactive power demand of the load changes, too. But this is of minor relevance here
because the changes are relatively small and hardly affect the current limits of the inverter.

\[
\text{Load : } P_L(V_i) = P_{L,0} \cdot \frac{V_i^2}{V_n^2} \quad (4.5)
\]

\[
\text{NCG : } P_{\text{NCG}}(\Delta f) = P_{\text{NCG,0}} \cdot \left(1 - \frac{0.4}{\text{Hz}} \cdot (f - 50.2 \text{ Hz})\right)
\]

\[
= P_{\text{NCG,0}} \cdot \left(1 - \frac{0.4}{\text{Hz}} \cdot \Delta f\right) \quad (4.6)
\]

In the Master, a droop is used which defines the new operating frequency dependent on the actual voltage level. \(\Delta f\) shall be at maximum if the voltage \(V_i\) reaches an upper limit \(V_{\text{max}}\) and zero as long as the voltage is below a certain limit \(V_{\text{lim}}\). This can be expressed by (4.7).

\[
\Delta f = (51.5 - 50.2) \text{ Hz} \cdot \frac{V_i - V_{\text{lim}}}{V_{\text{max}} - V_{\text{lim}}} \quad (4.7)
\]

By using (4.7) in (4.6), the desired frequency change \(\Delta f\) can be expressed as a function of the voltage. The NCG active power can thus be calculated as a function of the voltage and not only as a function of the frequency.

\[
P_{\text{NCG}}(\Delta f) \rightarrow P_{\text{NCG}}(V_i) = P_{\text{NCG,0}} \cdot \left(1 - 0.52 \cdot \frac{V_i - V_{\text{lim}}}{V_{\text{max}} - V_{\text{lim}}}\right) \quad (4.8)
\]

The new operating voltage \(V_{i,\text{new}}\) will be defined at the voltage level when \(P_L = P_{\text{NCG}}\), which is the intersection of (4.5) and (4.8) and can be calculated to:

\[
V_{i,\text{new}} = \frac{-0.52P_{\text{NCG,0}}V_n^2}{V_{\text{max}} - V_{\text{lim}}} \pm \sqrt{\left(\frac{0.52P_{\text{NCG,0}}V_n^2}{V_{\text{max}} - V_{\text{lim}}}\right)^2 + 4 \cdot P_{L,0}P_{\text{NCG,0}}V_n^2 \left(1 + \frac{0.52V_{\text{lim}}}{V_{\text{max}} - V_{\text{lim}}}\right)}
\]

\[
2 \cdot P_{L,0} \quad (4.9)
\]

With the new operating voltage, the new operating frequency reference value \(f^*_{\text{new}}\) can be calculated as a function of islanding voltage \(V_i\):

\[
f^*_{\text{new}} = \begin{cases} 
50 \text{ Hz} & \text{for } V_i < V_{\text{lim}} \\
50.2 \text{ Hz} + \Delta f & \text{for } V_{\text{lim}} \leq V_i \leq V_{\text{max}} \\
51.5 \text{ Hz} & \text{for } V_i > V_{\text{max}}
\end{cases} \quad (4.10)
\]

The respective curve is shown in Figure 4.11. The higher the voltage level, the higher the new reference value for the islanding frequency.

Figure 4.12 shows the voltage (a) and frequency (b) levels as a function of the ratio between the NCG power and the load demand. It can be seen that the natural limit for over-voltage is at the point where the load demand is 83% of the NCG power. By using the proposed control strategy and increasing the islanding frequency as shown in (b), this limit can be extended to a minimum load demand of 40% of the NCG power.

Figure 4.13 shows the functional chain of the proposed control. The Master measures grid RMS voltage \(V\) and compares it to the reference value \(V^*\). The controller computes the new reference value for the operating frequency \(f^*_{\text{new}}\). Finally the frequency controller changes islanding frequency. The NCG measures the frequency \(f_{\text{meas}}\) with its PLL and calculates the reference value for the active power output \(P^*(t)\) which is then fed into the island by the NCG current controller. The change in output power \(P(t)\) leads to a change in the islanding voltage \(V(t)\) which is measured by the Master unit.
Chapter 4. Novel Multiple Inverter Control Strategy

Figure 4.11: New frequency reference value $f_{\text{new}}^*$ as a function of islanding voltage $V_i$. $V_{\lim} = 1.03 V_n$, $V_{\max} = 1.10 V_n$.

Figure 4.12: New voltage (a) and frequency (b) operating points of the proposed control against the excess of active power. $V_{\lim} = 1.03 V_n$, $V_{\max} = 1.10 V_n$.

It should be noted that the frequency controller, the PLL and the plant have nonlinear transfer functions. This must be considered when designing the controller. The time constant $\tau_{50.2}$ of the first order lag element must be chosen slow enough to give the system some time to react and thus to prevent oscillations.

Figure 4.14 shows the results of a simulation with a Master and a NCG unit. Both have
4.4. Countermeasures against an Excess of Active Power

A nominal power of 10 kW. The load demand is 10 kW. First, the Master starts islanding operation. After 0.2 seconds, the NCG joins and increases its active power with 20 kW/s. At \( t = 1/1.5/2 \) s, the load is decreased by 15% (1.5 kW) each. This results in an increased voltage (a). The Master initiates a frequency change (b). The NCG reduces its active power (c) and thus the voltage level is stabilised below 1.1 pu. At \( t = 2.5/3/3.5 \) s, the load is increased by 15% (1.5 kW) each, which leads to a lower voltage. The Master reduces the islanding frequency and thus the NCG increases its power again. Finally, the frequency is stabilised at nominal value and the NCG can provide its full active power.

The short term overshoot in the voltage of Figure 4.14 (a) is due to the relatively large load steps. If the load changes more gradually, the transitions are smoother and the frequency control has enough time to slowly increase islanding frequency before the voltage reaches the upper limit. A fast control could reduce the voltage quicker but also reduces robustness of the control approach. Hence, a trade-off needs to be made. Besides, it might be suitable to set the upper frequency limit to a value slightly below 51.5 Hz. This could avoid accidental tripping of generators due to over-frequency. This is a trade-off because in this case, not the full potential for power reduction is used and this would lead to increased voltage. Maybe in summary this could result in better operability.

Compared to the state-of-the-art solution of the manufacturer SMA, the new solution has a drawback. With the use of the standard \( P(f) \) control curve it is not possible to reduce the NCG active power to zero. This can be seen in Figure 4.9. This is because the \( P(f) \) control is not intended to be used for a reduction to zero.
Figure 4.14: Simulation results of the proposed control against excess of active power. The reduction of the NCG active power output due to an increase in frequency can successfully be controlled with variations in the frequency reference values.
4.4. Countermeasures against an Excess of Active Power

Increase of Non-Controllable Generation

When the island was operated for at least 60 seconds and if the islanding voltage and frequency have been inside the limits, in accordance with the grid codes, NCG will rejoin. Because of their local voltage and frequency measurement they assume that grid parallel operation is possible again. At some point, the NCG might become larger than the load demand. In this case, the Master already reduced its active power to zero and cannot provide any further support to prevent the islanding voltage from rising.

Like in the previous case, the Master can increase the frequency above 50.2 Hz in case the voltage exceeds $V_{\text{lim}}$. According to the grid codes, the NCG active power must not be increased further as long as frequency is above 50.2 Hz and the excess of active power in the island can be stopped.

Theoretically, the NCG actual active power could be higher as long as the NCG slew rate is small enough and thus the Master has enough time to shift frequency above 50.2 Hz. Grid codes recommend a soft start procedure for generators with a maximum increase of active power $\frac{\Delta P_{\text{NCG}}}{\Delta t}$ of

$$\frac{\Delta P_{\text{NCG}}}{\Delta t} = \frac{10\%}{60 \text{ s}} \cdot P_{\text{NCG},n}$$

(4.11)

The additional NCG power that can be taken by the load inside the voltage limits can be calculated:

$$\Delta P_{\text{NCG}} = \frac{10\%}{60 \text{ s}} \cdot P_{\text{NCG},n} \cdot \Delta t = \left(\frac{V_{\text{max}}}{V_n}\right)^2 \cdot P_L$$

(4.12)

$$\Rightarrow P_{\text{NCG},n} = \frac{1.10^2 \cdot P_L \cdot 60 \text{ s}}{10\% \cdot \Delta t} = 726 \cdot \frac{P_L \cdot s}{\Delta t}$$

(4.13)

Thus, the time constants for the control of frequency change could be selected relatively slow. On the one hand, this could be better to prevent oscillations and interactions with other control algorithms. On the other hand, the method would be more prone to transient events. This is important for relatively large load steps as was shown in the previous paragraph.

With a time constant $\Delta t = 10 \text{ s}$, the Master could control NCG that has approximately 73 times the active power of the load. Some inverter manufacturers have implemented so called soft-start parameters in order to not disturb the grid too much when reconnecting to the grid. Of course, dependent on the actual grid codes and the parameters given by the manufacturers, those values may vary. As an example, SMA provides a set of parameters in [90].

Figure 4.15 shows the simulation results of an increase of active power by NCG. In the beginning, the Master starts islanding operation and provides the necessary active power. After $t = 0.2$ seconds, the NCG joins the island and constantly increases its active power with 5000 W/s. When there is an excess of active power at about $t = 1.7$ s, the Master raises the islanding frequency above 50.2 Hz (here: 50.75 Hz). This immediately stops the NCG power increase and the increase in voltage is stopped. The faster the increase in active power and the large the time constant of the frequency change, the higher the steady-state voltage level will be. This can be seen from (4.11)–(4.13).

The concept can also be used if there are multiple Followers in the network. Like the Master, they will reduce their active power to zero and remain at zero power operation during the whole process. The increase in frequency is initiated by the Master without disturbance of the Followers as discussed in the previous subsection.
Figure 4.15: Simulation results of the proposed control against excess of active power. An increase of active power is successfully stopped by shifting the frequency above 50.2 Hz.
4.5 Experimental Validation

The setup for the validation of multi-inverter operation is analogue to the setup of chapter 3. Figure 4.16 shows an equivalent circuit of the test setup. Dependent on the test scenario, either two Master/Follower are used or one Master/Follower and one NCG. The load is a parallel \(RLC\) circuit. The results are presented on pages 89 to 91.

4.5.1 Procedure from Zero-Voltage and Adaptation to Load Conditions

Figure 4.17 shows the experimental results of the coordinated procedure from zero-voltage condition. The values for the setup can be found in Table 4.3. At \(t = 0\) s, the first inverter determines itself as the Master and starts energising the island. As it can only provide 4 kW, but the load demands for 5.8 kW, it is not able to establish the nominal voltage level. The voltage saturates at \(V \approx \sqrt{\frac{4000}{5800}} \cdot V_n = 0.83\) p.u. After the delay time \(t_{\text{delay}} = 0.1\) s, the Follower joins and supports the Master by providing the lacking amount of active power. At \(t = 0.17\) s, the nominal voltage level is reached and the Follower disables its integral control part as shown in Figure 4.17 (a). At \(t = 0.35\) s, the load is reduced to 2 kW and to 0 kW at \(t = 0.41\) s (open circuit condition). In both cases, the Master and Follower react to the short voltage overshoot and immediately reduce their active power. Both transients are shorter than the fundamental period (20 ms) which means, that voltage quality is still relatively good. Figure 4.17 (c) and (d) zoom into the transient response during the load steps. At \(t = 0.64\) s, the load is reconnected. After a short voltage sag to 0.6 p.u. for about 20 ms, the voltage can be restored conjointly by the two inverters.

One should notice that after the open circuit condition, the active power sharing between the Master and the Follower is different from the initial one, as shown in Figure 4.17 (b). With regard to control stability, it is not of importance, which of the inverters provides which amount of active power, as long as the sum is equal to the load demand and only the Master has its integral part activated. As it can be seen, at \(t = 0.66\) s, the Follower deactivates its integral part as soon as nominal voltage is reached. In fact, the power sharing depends on the output impedance which depends on the design procedure of chapter 3 and is a function of the nominal power of the inverters.

If the number of inverters is large, the Master’s share can be relatively small. Although not demonstrated in experiments, the joining of numerous Followers can still result in reaching the nominal voltage within 200 ms. As every voltage control loop can be designed with the same
Chapter 4. Novel Multiple Inverter Control Strategy

Table 4.3: Parameters for experiment of procedure from zero-voltage condition and load adaptation.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_M$</td>
<td>Active power of the Master</td>
<td>4 kW</td>
</tr>
<tr>
<td>$P_F$</td>
<td>Active power of the Follower</td>
<td>2.5 kW</td>
</tr>
<tr>
<td>$P_L$</td>
<td>Active power of the load</td>
<td>5.8</td>
</tr>
</tbody>
</table>

The islanding system behaves like it was discussed in chapter 2. Active and reactive power consumption are in accordance with the equations. The controller design of chapter 3 was based on a large-signal analysis which is based on the connection between active power and voltage and the connection between reactive power and frequency. It might suffer from a different small-signal behaviour if motor loads are connected during islanding operation. In this case, there is an additional coupling between active power and frequency and between reactive power and voltage. Thus, a superposition of $RLC$ and motor loads will determine the transient voltage and frequency behaviour. This will have major effects on the control stability and requires future research.

4.5.2 Compensation of a Master Outage

Figure 4.18 shows the results of an experiment in which the Master inverter trips at $t_0 = 0.5$ s. The values for the experiment can be found in Table 4.4. The event leads to deviations in both voltage in Figure 4.18 (a) and frequency in Figure 4.18 (b). The Follower immediately stabilises the island with its proportional control. As soon as voltage and frequency deviations violate the dead-band, the integral terms (both voltage in (a) and frequency in (b) ) are activated and drive the error to zero. This is done by providing the necessary active and reactive power as shown in Figure 4.18 (c). After $t_{f_{stable}} = 1$ s, the Follower’s integral term is deactivated again. Naturally, there are some transients in both the voltage and frequency after the Master has tripped. But the transients can be handled very quickly as shown in Figure 4.18 (d).

Table 4.4: Parameters for experiment of Master outage compensation.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_M$</td>
<td>Active power of the Master</td>
<td>4 kW</td>
</tr>
<tr>
<td>$P_F$</td>
<td>Active power of the Follower</td>
<td>3 kW</td>
</tr>
<tr>
<td>$P_L$</td>
<td>Active power of the load</td>
<td>2 kW</td>
</tr>
<tr>
<td>$C_L$</td>
<td>Load parallel capacitor for reactive power</td>
<td>20 µF</td>
</tr>
<tr>
<td>$f_n$</td>
<td>Nominal frequency</td>
<td>50 Hz</td>
</tr>
<tr>
<td>$\Delta V$</td>
<td>Voltage deviation when integral control is activated</td>
<td>0.05 p.u.</td>
</tr>
<tr>
<td>$\Delta f$</td>
<td>Frequency deviation when integral control is activated</td>
<td>1 Hz</td>
</tr>
</tbody>
</table>
voltage drop is shorter than 20 ms and thus is not assumed to be a problem for most of the loads.

Although an outage of the Master can be handled, new questions arise with regard to long-term operation. After the Follower disables its integral term of frequency controller, the islanding frequency will not be fixed to nominal value any longer. From this moment, frequency will face deviations. If the deviations finally exceed the frequency dead-band (here 1 Hz), the Followers will again drive back the frequency to nominal value. But in the long run, this state might not be very desirable. In this case, a long-term solution needs to be developed. There are several possibilities: The frequency dead-band could be gradually reduced to attenuate the frequency changes. Or the Followers decide to define themselves as Master units if the frequency dead-band has been violated for too many times. But then it has to be sure that there are not two Followers becoming the new Master at the same time because then two integral controller terms would be active simultaneously. This could be prevented by considering the nominal power of the inverters like in the start-up procedure. The next best Master would be the Follower with the highest nominal power rating. Thus, Followers could measure the rate of violations of the frequency dead-band within a certain window period and decide to become the new Master the sooner the higher their nominal power rating. Another possibility would be using a proportional term to at least limit the frequency deviations to a minimum. This would incorporate a frequency droop control. But the design of the proportional term could be very challenging because the system gain $K_{S,f}$ which describes the connection between reactive power and frequency strongly depends on the reactive components in the grid. This was shown in section 2.3.

### 4.5.3 Islanding with Non-Controllable Inverters

Figure 4.19 shows the results for an islanding operation with one Master and one NCG inverter. The power ratings of the inverters are provided in Table 4.5. The NCG would provide twice as much active power as it is needed by the load. Thus, if there is no control, the voltage would finally exceed $V_{\text{max}} = 1.1$ p.u. and the island is not able to survive in the long run. But with the new control solution, the NCG can be controlled indirectly by the Master by changing the frequency. It should be noted, that the actual slew rate and waiting time of the NCG $t_{\text{rec}}$ have been adapted in order to provide a convenient illustration of the results.

After the Master has established islanding operation, the NCG joins after $t_{\text{rec}} = 1$ s and increases its active power with $\Delta P_{\text{NCG}} = 500 \, \text{W} \cdot \text{s}^{-1}$. When the NCG increases its active power, the Master reduces its injection in order to keep the voltage at the desired value, see Figure 4.19 (c). The Master finally reduces its power to zero but the NCG injection still rises, which increases

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_M$</td>
<td>Active power of the Master</td>
<td>2 kW</td>
</tr>
<tr>
<td>$P_{\text{NCG}}$</td>
<td>Active power of the NCG</td>
<td>4 kW</td>
</tr>
<tr>
<td>$P_L$</td>
<td>Active power of the load</td>
<td>2 kW</td>
</tr>
<tr>
<td>$\Delta P_{\text{NCG}}$</td>
<td>Slew rate of the NCG</td>
<td>500 W s$^{-1}$</td>
</tr>
<tr>
<td>$V_{\text{max}}$</td>
<td>Upper voltage limit</td>
<td>1.1 p.u.</td>
</tr>
<tr>
<td>$V_{\text{lim}}$</td>
<td>Voltage level when limitation starts</td>
<td>1.05 p.u.</td>
</tr>
</tbody>
</table>
the voltage, as shown in Figure 4.19 (a). At $t = 5.4$ s, the voltage exceeds the control limit $V_{\text{lim}} = 1.05$ p.u. and the frequency changing by the Master is activated. At $t = 5.6$ s, the 50.2 Hz limit is reached and the NCG immediately stops increasing the active power, as shown in Figure 4.19 (c). Finally, an operating point is reached at about $V = 1.06$ p.u. and $f = 50.4$ Hz. The results of Figure 4.19 show that the indirect control of any NCG by controlling the islanding frequency is effective and applicable for NCG that is even larger than the Master itself.
Figure 4.17: Experimental results for the procedure from zero-voltage condition using a Master and a Follower: (a) voltage curve and times when the Follower activates its integral term, (b) active power provided by Master $P_M$ and Follower $P_F$, (c) frequency, (d) and (e) transient voltage during load steps of (a).
Figure 4.18: Experimental results for a compensation of an outage of the Master and a take-over of the Follower which stabilises voltage (a) and frequency (b) by providing the necessary active and reactive power (c). Transient voltage dips are shown in (d).
4.5. Experimental Validation

Figure 4.19: Experimental results for the limitation of NCG output power by a frequency change. (a) RMS voltage, (b) active power of Master $P_M$ and NCG $P_{NCG}$, (c) frequency. Left dotted-dashed line marks the activation of the frequency-change, right dotted-dashed line marks the limitation of the NCG due to excess of frequency limit at 50.2 Hz. The time delay is a function of the time constant $\tau_{50.2}$. 
Chapter 5

Grid Integration and Compatibility

In this chapter, some key requirements regarding compatibility of islanding operation and its grid integration are discussed. A novel concept is proposed which allows the conjoint implementation of low-voltage ride-through capability (LVRT), anti-islanding detection (AID) by a time decoupling. With the help of a case study, the proposed concept is tested in relevant cases. Besides, the implementation of intentional low-voltage islanding operation subsequently LVRT and AID is proposed by incorporating the control strategies of the previous chapters. For sure, grid integration will be one of the big challenges of islanding operation. Thus, open questions and problems that have not been investigated in this thesis are addressed in the end.

5.1 Conflicting Aims of AID, LVRT and Islanding Operation

The requirements of intentional islanding operation, AID and LVRT are antithetic, as shown in Figure 5.1. Intentional islanding operation must not undermine the detection of unintentional islanding because this might cause hazards for human beings and generators in case of asynchronous reconnection. Furthermore, it must be possible to provide LVRT during faults in order to support local voltage recovery and local grid stability.

![Figure 5.1: Conflicting aims of intentional islanding operation, anti-islanding detection (AID) and low-voltage ride-through (LVRT).](image-url)
The aims of Figure 5.1 are paraphrased and ranked according to their relative importance with regard to low-voltage grids:

1. protection of generators and other facilities of the grid,
2. protection against local voltage collapse,
3. shut-down of unintentional islands due to various hazards,
4. initialisation of intentional islanding operation

The protection of generators and facilities of the grid has the highest priority. During abnormal grid conditions they are more vulnerable to damages than during normal operation. Thus, protection is most important during faults. Distributed generation in low-voltage grids is mainly inverter-based. Besides over-voltages, high currents are hazardous to power electronics. Inverter-based generation is usually current controlled [75]. Thus, it can be much better protected against over-currents. Hence, inverters can stay connected to the grid with a relatively low risk of damages caused by asynchronous reconnection.

Due to the relatively high level of controllability and protection, the LVRT requirements for inverter-based generation are higher than for synchronous generation [47]. Because of this, in [47] and [48], new window periods for LVRT have been proposed. In high- and medium-voltage grids, where LVRT has originally been used, AID has not been an issue yet. Thus, it might not be suitable to transfer the requirements from higher grid levels to low-voltage grids without analysing the interactions that might come from AID.

One of the key recommendations in [47] and [48] was that it is absolutely vital to investigate whether the effectiveness of AID is undermined by the implementation of LVRT. This issue is also crucial for the implementation of intentional islanding operation in low-voltage grids. Only if unintentional islanding is avoided and if inverters in low-voltage grids are still able to contribute to local voltage recovery and stability, the implementation of intentional islanding operation might be useful and might not be at the expense of the utility grid.

In this thesis, a novel concept for the conjoint implementation of LVRT, AID and intentional islanding in inverter-based generation is proposed. It is composed of two parts. The first part implements a new LVRT algorithm and provides proof that it does not undermine the effectiveness of AID in low-voltage grids by applying a case study (section 5.2). The second part demonstrates that the novel control concepts of chapters 3 and 4 could be used to implement intentional islanding operation subsequently to an effective delivery of LVRT and AID capability.

Figure 5.2 illustrates the sequence that incorporates the proposed concept for the conjoint implementation of LVRT, AID and intentional islanding. At $t = t_0$, the fault occurs and the voltage drops. Inverters provide LVRT capability. If the fault cannot be cleared, voltage will eventually drop below the minimum LVRT curve ($t_1$). Inverters do not need to support the grid any longer but they trip. After the shut-down ($t_2$), the procedure from zero-voltage condition is triggered and finally intentional islanding operation starts ($t_3$).
5.2 Novel Concept for the Compatibility of AID and LVRT

Figure 5.3 illustrates the actual implementation of the novel concept of simultaneous AID and LVRT capability. It includes the proposed LVRT borderline that will become mandatory for inverter-based generation in Germany which was shown in Figure 2.15 on page 27. The inverter must not trip when voltage drops below 80% of nominal voltage in at least one phase. In that case, the inverter switches to LVRT mode. Instead of tripping it provides reactive current.

\[ V_{g,RMS}(t) < 80\% V_n \] in at least one phase

LVRT mode activated

while \( t < 2 \text{ s} \)

\[ V_{g,RMS}(t) > V_{LVRT}(t) \] (in all phases)

no

LVRT mode (no active AID)

trip

\[ V_{g,RMS}(t) > 85\% V_n \]

no

yes

normal operation

inverter trips

Figure 5.3: Novel LVRT algorithm for combining AID and LVRT capability. When LVRT mode is activated, constant voltage monitoring determines whether the actual voltage \( V_{g,RMS}(t) \) is above the minimum required LVRT voltage \( V_{LVRT}(t) \) from Figure 2.15 in all phases. If \( V_{g,RMS}(t) < V_{LVRT}(t) \), the inverter is allowed to trip. After the LVRT event and if \( V_{g,RMS}(t) > V_{LVRT}(t) \) \( \forall t \), the inverter returns to normal operation [91].
Chapter 5. Grid Integration and Compatibility

LVRT mode has been activated

1. Islanding with voltage above 80% $V_n$
2. Islanding with voltage below 80% $V_n$
3. Voltage drop and ordinary LVRT event
4. Voltage drop violation of LVRT curve
5. Misinterpretation of voltage drop

**Figure 5.4:** Case study: behaviour of the islanded system in each of the five cases that are investigated for effective implementation of LVRT and AID [91].

From the moment when LVRT mode is activated, the voltage level is constantly monitored and compared to the curve shown in Figure 2.15. If the lower voltage limit is exceeded in at least one phase, the inverter is allowed to trip. When voltage recovers to above 85%, the inverter returns to normal operation. Tripping from the grid is allowed if frequency limits (47.5 Hz ... 51.5 Hz) are exceeded as this is a clear indicator for islanding [91].

### 5.2.1 Case Study

In order to prove that the proposed algorithm of Figure 5.3 provides good results in the relevant cases, five cases need to be examined as shown in Figure 5.4. It has to be checked for each one whether the inverter’s behaviour is as desired:

1. Islanding with voltage above 80% nominal voltage,
2. Islanding with voltage below 80% nominal voltage and thus possible misinterpretation as grid fault requiring LVRT behaviour,
3. Voltage drop (no islanding) without violation of the LVRT curve of Figure 2.15 and voltage recovery above 85% $V_n$,
4. Voltage drop (no islanding) with violation of the LVRT curve of Figure 2.15 or voltage recovery below 85% $V_n$,
5. Voltage drop misinterpreted as islanding and inverter tripped.

**Islanding with voltage above 80% nominal voltage:** If active power generation and consumption are balanced when an island originates, voltage does not drop below 80% $V_n$. Thus, LVRT mode is not activated and AID stays in effect. As described in section 2.6, usually active methods such as active frequency shifting are implemented and able to detect islanding [65,92]. If methods are used that perturb the islanding voltage, the next case has to be investigated.

**Islanding with voltage below 80% nominal voltage:** If islands originate without sufficient active power generation, voltage drops below 80% $V_n$ and thus LVRT mode is activated. The inverter only provides reactive power. Eventually, voltage will break down completely. As this violates the curve of Figure 2.15, the inverter will trip and the island can be detected effectively. If the inverter also injects active current/power during an LVRT event (which is not discussed here) there is a chance that voltage does not collapse that fast, but still stable operation is very
unlikely due to the high transients in both active and reactive power. Actual grid codes stipulate reactive current only which is why this case is investigated and shown here.

**Voltage drop with and without violation:** In both cases, the inverter operates with the desired properties according to the requirements of LVRT capability.

**Misinterpretation of voltage drop:** In the past, voltage drops always led to inverters disconnecting because it was mandatory due to the grid codes. Because of this, inverters were not available for further grid support. Activating LVRT mode would mean that disconnection is not permitted and dynamic grid support through injection of reactive power is mandatory. Those generators would then still be available to support the grid. Tripping thus does not occur with the proposed algorithm. As this case is actually a sub-case of a voltage drop without violation of the LVRT curve, it is not discussed further.

### 5.2.2 Asymmetrical Conditions

Asymmetrical load conditions are less critical for islanding detection than symmetrical ones. As soon as one of the phases violates the voltage limits, detection takes effect and the inverter trips. Furthermore, the frequency deviations increase and thus frequency detection based on active frequency shifting is still effective. This is why a symmetrical RLC resonant circuit is always mandatory for standard anti-islanding tests in all three phases.

During unbalanced faults, the provision of low-voltage ride-through capability is more challenging. In unbalanced systems, the Park transformation does not provide constants for voltages and currents in the synchronous reference frame. Thus, voltages and currents have to be decomposed into their positive and negative sequence components as shown in Figure 5.5 (a) [93–97].

Natural voltage $v_{abc}$ and natural current $i_{abc}$ are decomposed in their positive ($v_{abc}^+$, $i_{abc}^+$) and negative sequence ($v_{abc}^-$, $i_{abc}^-$). The positive ($\omega^+$) and negative ($\omega^-$) Park transformation results in the positive and negative synchronous reference frame values for voltage and current $v_{dq}^+$, $v_{dq}^-$, $i_{dq}^+$, $i_{dq}^-$. 

![Figure 5.5: (a) decomposition of voltage and current into positive and negative sequence components, (b) control of both positive and negative sequence currents to the respective reference values $i_{dq}^+$ and $i_{dq}^-$ [91].](image-url)
The decomposition leads to constant current reference signals for the current controller in synchronous reference frame. Thus, the PI current controllers can provide the modulation signals \((m_{dq}^+, m_{dq}^-)\) which can be transformed into natural modulation signals \(m_{abc}\) with the inverse Park transformation. This is shown in Figure 5.5 (b).

5.2.3 Simulation Results for Representative Test Cases

In the following, simulation results will be shown for each of the five cases. Figure 5.6 shows the general setup. A three-phase inverter is connected to the grid via an LC filter and a transformer. At the point of common coupling, a resonant RLC load is connected which will be used to form stable islands. The DC side of the inverter is simulated using a single-diode model of a PV array [98]. For experimental validation in the laboratory, a constant voltage source is used. If active power is reduced to zero during LVRT mode, the DC-link voltage will rise. Hence, two possible schemes for protection against over-voltage are implemented. A switch \(S_M\) can disconnect the PV array from the DC-link capacitor. The second protection scheme is a chopper resistance \(R_{ch}\). When switch \(S_{ch}\) is closed, active power can be dissipated in the chopper. The parameters that were used for simulation can be found in Table 5.1.

Active power consumption of the RLC load was set to: \(P = P_{inv \cdot 0.92}\), \(P = P_{inv \cdot 0.72}\) and \(P = P_{inv}\). The quality factor \(Q_i\) is set to 1. The results are presented on pages 100 to 104.

Islanding with voltage above 80% nominal voltage: The result is shown in Figure 5.7. When the system is islanded at \(t_0 = 0.05\) s, the island will be destabilised by the active AID method. Although voltage decreases slightly, the frequency change is much quicker. Thus, the frequency limits are exceeded and the inverter is tripped.

Islanding with voltage below 80% nominal voltage: Figure 5.8 shows the result of the simulation. After islanding, voltage drops below 80%. This activates the LVRT mode. Thus, active power is reduced to zero and voltage drops further. The transients in active and reactive power disturb both islanding frequency and voltage. Eventually either the LVRT curve of Figure 2.15 or the frequency limit is violated and the inverter trips.

Voltage drop without violation of the LVRT curve: The results are shown in Figure 5.9. In the beginning, the inverter injects 2 kW. At \(t_0 = 0.05\) s, grid voltage drops below 80% \(V_n\) (a). It remains above the requested voltage curve throughout the test. The inverter switches to LVRT mode until grid voltage exceeds 85% \(V_n\) again at \(t_2 = 1.6\) s. During LVRT, active power

---

**Figure 5.6:** Single-phase equivalent Circuit for the simulation and experimental results for simultaneous implementation of LVRT, AID and intentional islanding operation, modified from [91].
Table 5.1: Components and settings for grid simulation setup of conjoint implementation of LVRT and AID.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_n$</td>
<td>Nominal grid voltage</td>
<td>230 V</td>
</tr>
<tr>
<td>$f_n$</td>
<td>Nominal grid frequency</td>
<td>50 Hz</td>
</tr>
<tr>
<td>$f_{PWM}$</td>
<td>PWM frequency</td>
<td>10 kHz</td>
</tr>
<tr>
<td>$V_{DC}$</td>
<td>DC voltage</td>
<td>750 V</td>
</tr>
<tr>
<td>$r_T$</td>
<td>Transformer ratio</td>
<td>230/100 V</td>
</tr>
<tr>
<td>$L_F$</td>
<td>Combined filter and transformer inductance</td>
<td>25 mH</td>
</tr>
<tr>
<td>$R_F$</td>
<td>Combined filter and transformer resistance</td>
<td>60 mΩ</td>
</tr>
<tr>
<td>$C_{DC}$</td>
<td>DC capacity</td>
<td>1100 µF</td>
</tr>
<tr>
<td>$\tau_i$</td>
<td>Current control time constant</td>
<td>4 ms</td>
</tr>
</tbody>
</table>

is reduced to zero, see Figure 5.9 (b) and (c). The excess of active power causes an increase in DC link voltage (d) and hence protection is activated. Either the switch $S_M$ disconnects the PV array or the chopper resistance is used to dissipate power. In this case, the PV panel is disconnected and voltage decreases. Changes in DC-link voltage have only marginal effects on the current and power control loop.

**Voltage drop with violation of the LVRT curve:** Figure 5.10 shows the simulation results for a voltage drop below the LVRT curve. Initially, the inverter changes active and reactive currents as intended but when voltage violates the lower limit, the inverter trips.

**Misinterpretation of a voltage drop as an islanding event:** This case is a sub-case of a voltage drop without violation of the LVRT curve. Thus, the behaviour is analogue to Figure 5.9.

**Asymmetrical Conditions:** Figure 5.11 shows the LVRT behaviour of the inverter for an asymmetrical fault. LVRT mode is activated and the inverter controls its active currents $i_d^+$ and $i_d^-$ to zero and increases the positive sequence reactive current $i_q^+$. Thus, the grid currents are relatively balanced as shown in (b). Active power is controlled close to zero apart from small oscillations as can be seen in (d). Due to unbalanced voltages, the PLL faces some transients but recovers quickly.
Figure 5.7: Islanding with voltage above 80% of nominal voltage: simulation of a successful detection of a stable island by using a standard slip mode frequency shift algorithm. The LVRT-mode is not activated.
5.2. Novel Concept for the Compatibility of AID and LVRT

Figure 5.8: Islanding with voltage below 80% nominal voltage: simulation of a breakdown of voltage if generator applies reactive power only to a parallel RLC load.
Figure 5.9: Voltage drop without violation of the LVRT curve: simulation test of the LVRT algorithm for a valid voltage drop that is constantly above the lower LVRT-limit and thus determines the inverter to provide LVRT capability. The protection devices on the DC-link side keep the DC voltage below the upper limit.
5.2. Novel Concept for the Compatibility of AID and LVRT

Figure 5.10: Voltage drop with violation of the LVRT curve: simulation test of the LVRT algorithm for a voltage drop that violates the lower limit of the LVRT curve and thus leads to tripping of the inverter.
Figure 5.11: Asymmetrical low-voltage event in phase A at $t_0 = 0.05$ s, decomposed current components can be controlled as intended, active and reactive power remain relatively balanced.
5.2.4 Experimental Validation

In the following, simulation results are validated by experiments. As shown in Figure 5.6, the PV model is replaced with a constant DC voltage source. The results are presented on pages 105 to 108.

**Islanding with voltage above 80% nominal voltage:** Figure 5.12 shows the experimental validation. The AID method is able to shift the frequency within 20 ms and the inverter is tripped very fast.

**Islanding with voltage below 80% nominal voltage:** Experimental validation is shown in Figure 5.13. The voltage drop at \( t = 0.05 \) s activates the LVRT mode. The inverter tries to provide reactive current but due to the high transients in both voltage and frequency, islanding can be detected successfully and the inverter is tripped.

**Voltage drop without violation of the LVRT curve:** Figure 5.14 shows a voltage drop to 50% \( V_n \). During the fault, the inverter remains in LVRT mode. After voltage has recovered, the inverter switches back to normal operation.

**Voltage drop with violation of the LVRT curve:** Figure 5.15 shows the results for this case. Voltage remains above the LVRT curve within the first 300 ms. Eventually, the limit of \( V_{LVRT}(t) \) is violated, the inverter stops injecting reactive current and is tripped.

---

**Figure 5.12:** Islanding with voltage above 80% nominal voltage: experimental results for an islanded system at \( t_0 = 0.05 \) s. The effectiveness of the active frequency shifting is not weakened and the island can be detected.
Figure 5.13: Islanding with voltage below 80% nominal voltage: experimental results for an islanded system at $t_0 = 0.05$ s with less active power that would result in a voltage below 80% of nominal value. Effective frequency detection is even quicker than voltage detection and trips the inverter.
5.2. Novel Concept for the Compatibility of AID and LVRT

Figure 5.14: Voltage drop without violation of the LVRT curve: experimental results of applying an LVRT event with a voltage drop to 115 V. The inverter successfully provides reactive current throughout the event.
Figure 5.15: Voltage drop with violation of the LVRT curve: experimental results of applying an LVRT event with a voltage drop to 80 V. The inverter provides reactive current as long as the voltage is above the $V_{\text{LVRT}}(t)$ curve. After violation, the inverter trips.
5.3 Demonstration of Subsequent Islanding Operation

In the previous sections it was shown that the detection of LVRT events and islanding can be accomplished. In the following, the transition from shut-down ($t_1\ldots t_2$) to intentional islanding operation ($t_2\ldots t_3$) will be demonstrated.

In the previous section, the inverter tripped when grid voltage dropped below the level of the LVRT borderline. Instead of waiting for the grid to recover and eventually re-starting grid parallel operation, the inverter will now start islanding subsequently to tripping.

The setup of Figure 5.6 is used for experimental validation (constant voltage source). The inverter is equipped with the voltage and frequency control loop of chapter 3, the procedure from zero-voltage condition of chapter 4 and with the LVRT-capability algorithm of section 5.2.

Figure 5.16 shows the test sequence for subsequent intentional islanding operation after a possible fault in the medium-voltage grid. In the beginning, the inverter is operating with constant active and reactive power (5 kW and -1 kvar). At $t = 0$, the voltage drops and the LVRT mode is activated (illustrated by the control and status signals). Positive reactive current is injected and active power is reduced to zero. After 300 ms, voltage drops below the LVRT borderline and the inverter trips. The disconnection device to the medium-voltage grid is opened, voltage collapses and the system is islanded. During $t_{rec}$, the inverter is processing the procedure from zero-voltage condition and at $t = 0.36$ s, intentional islanding operation is initiated. The nominal voltage level is reached and the local load is supplied with the necessary active and reactive power which differs from the initial values.

The implementation of the proposed concept requires that the disconnection device of Figure 5.6 disconnects the utility grid within a certain window period. This could for example be incorporated with a voltage and frequency measurement on both sides of the switch. The proposed LVRT curve for low-voltage grids can be compared to the actual voltages (like in the inverter) and in case the voltage limits are violated, the switch trips. This ensures a disconnection of the utility grid before initialisation of islanding operation.
Figure 5.16: Test sequence for subsequent intentional islanding operation after a possible fault in the medium-voltage grid and subsequent opening of the disconnection device [22].
5.4 Open Issues and Future Challenges

Integration of intentional islanding operation will be a challenging task in the future and requires ongoing research. There are several issues and problems that have not been discussed in this thesis or have been simplified for modelling purposes. Some of them are discussed in the following to provide an outlook.

**Single inverter operation:** The new controller design for single inverter operation was mainly based on the equations for linear and symmetrical loads. Although stable controllability was also demonstrated for nonlinear constant power loads, the limitations grew apparent. Generally, the higher the share of nonlinear loads, the more challenging it is to maintain stable voltage and frequency control loops. This is due to the fact that the equations for linear loads do not fully apply and because of further non-ideal conditions, such as harmonics or asymmetrical loads. Recent research has presented various methods to improve controllability by introducing specially designed islanding control loops that use the potential of optimised hardware and software setups which might be superior to unified controller design approaches in some cases. Because of this, control robustness of the new proposed voltage and frequency controller design method should be proven under more realistic conditions in field tests in the future. This is crucial to evaluate if the robustness of unified controller design approaches is sufficient for the variations in low-voltage grids.

With regard to harmonic compensation, effective countermeasures against harmonics are in the focus of research on inverter-based generation. Harmonics can be attenuated by integrating harmonic load current feed-forward signals or by shaping the inverter output impedance to make the inverter behave like a resistor for high-frequency currents [99–106]. Additionally, particular attention should be paid to asymmetrical load conditions because this is a common problem in low-voltage grids. The problem is in the focus of research. The basic approach is to decompose grid voltages and currents into their positive and negative sequence components and control each of them separately [93–97]. With this, negative sequence components can be controlled to zero and positive sequence components can be controlled to their reference values. This approach has also been used in chapter 5 for the controllability of asymmetrical faults. Therefore it might be better to use a three-phase four-leg architecture in order to provide simultaneous supply for each phase individually [97]. The problem of asymmetrical conditions becomes even more important when single-phase loads and single-phase inverters are included into the system.

Besides, motor loads have been neglected in this work. Motor loads must trip automatically in the event of a voltage drop and they must not re-connect automatically but manually. Thus, the transient start-up from zero-voltage condition might be less prone to the effects of motor loads in the beginning. But when they are re-connected after some time, their transient behaviour might be challenging for the proposed control approach. Furthermore, the coupling of active power and voltage and the coupling of reactive power and frequency is changed significantly which could have major effects on the small-signal behaviour and thus the controllability of the system. In this case, small-signal and large-signal behaviour differ strongly which could be challenging for the large-signal approach that was presented in this thesis. This could also be the case if synchronous generators join the islanded system as non-controllable generation units. They impose similar transient behaviour as motor loads. The existence of synchronous generation in an island will also have an effect on the multiple inverter operation strategy.

**Multiple inverter operation:** In this thesis, the focus of multiple inverter operation has been on the potential of robust control without communication. Robustness of the control also relies
on a clear determination, which inverter unit takes the lead and becomes the Master unit. On the one hand, there are further issues for the interaction between controllable inverters. In future research it should be clarified what are the chances of two inverters becoming Master at the same time. This mainly depends on the actual low-voltage grid structures and the amount of generators that are connected to a single island. And if there are multiple Masters in an island, it must be investigated, whether there are severe effects that prohibit islanding operation. Maybe there is a steady-state power sharing between two Master units although both of them operate with integral voltage and frequency controllers. In case of an outage of the Master, a Follower must take the Master’s role in the island. As explained previously, in this case frequency control requires attention because it needs to be decided which of the Followers will become responsible for frequency stability.

The effects of non-controllable generation (NCG) and the novel countermeasures that have been presented in this work must be validated for different types of NCGs in the future. In case, a NCG is a rotating generator, it will be more challenging for the Master to change the islanding frequency in case there is an excess of active power that would lead to an over-voltage violation. Another issue with regard to NCG is active anti-islanding detection such as slip mode frequency shifting. If NCG constantly tries to destabilise the island, the frequency stability might be endangered. Certainly, this depends on the ratio of controllable and non-controllable generation and the limits should be identified in future research. Besides, future grid codes will affect even islanding behaviour of NCG as it was shown in [70]. This could have an effect on both the transient and the steady-state behaviour.

Grid integration: The most challenging task for intentional islanding operation might be a safe and reliable grid integration concept. Therefore, many partners such as grid code committees, distribution system operators and manufacturers need to define rules and a suitable framework. But also with regard to the islanding control strategy, there are definite open issues. This work provided a novel start-up sequence. But like for microgrids, a re-synchronisation process is essential to combine the benefits of both operation modes. The re-connection of islanded grids is in the focus of research and there is extensive study on suitable algorithms [107–111]. The main concept is to measure islanding and grid voltage and slowly reducing the phase and frequency difference with an integral controller. The difference in voltage is also reduced slowly with an integral controller. The usage of this concept might be contradictory to the proposed Master-Follower approach because there is no communication and thus the inverters do not know when to initiate the re-synchronisation process. Another option is to wait for an accidental alignment of voltage and frequency followed by a quick re-connection [87]. This method is based on timing and does not rely on controllability of inverters. This might be a promising approach and could be part of the disconnection device which is required to create islanded grids. But this could lead to multiple Masters in a single island and still the Master and Follower units must be able to detect that they are not operating in an island but in grid parallel.

Maybe a more promising approach would be the controlled shut-down of the inverters prior to a re-connection to the utility grid. This shut-down could be initiated internally by the Master and Followers or externally. A key to an external provocation of the shut-down would be to intentionally violate the non-detection zone that was presented in section 2.6. The inverters must shut down if either voltage or frequency violate their limits. Theoretically, this could be accomplished with remote anti-islanding detection methods. For example with the help of big capacitors which would shift islanding frequency below the lower limit of 47.5 Hz, hence leading to a shut-down of the inverter. But some of these approaches might not be very economic if the number of separated islands is relatively large.

A controlled shut-down procedure is even more of importance when islanding operation must
be prohibited by all means for example during maintenance work. If a part of the grid is disconnected and shut-down, it must not initiate islanding operation which could lead to risks to maintenance personnel. Besides it must be considered what needs to be done if the start-up procedure of chapter 4 fails the first time. If there are further attempts, the synchronisation and determination of the Master unit might become even more challenging. Besides, it is not clear when to start further attempts and when this would be useful or even dangerous. Maybe it would be better not to take further attempts due to safety reasons. But in this case, the potential of islanding operation might remain unused.

Finally, suitable protection schemes are crucial for the implementation of islanding operation in the field. Protection devices in combination with inverter-based generation is more prone to a reduced level of short-circuit currents. Thus, new protection concepts might be necessary to allow safe operation during and subsequently to fault conditions inside the island.
Chapter 6

Conclusions and Outlook

Distributed generation (DG) has been on the increase in the last decades. Especially in low-voltage grids, the number of inverter-based generation is very high and there are parts of the grid which face a temporary excess of active power, resulting in a reverse energy flow. Whereas in the past, this reverse energy flow was challenging because this could lead to unintentional islanding, nowadays this offers additional potential. These grids theoretically could provide intentional islanding operation independent of the rest of the utility grid. But the majority of the installed generators is not able to provide islanding operation because it is not equipped with the necessary voltage and frequency control loops.

Thus, the objective of this thesis was to provide a novel voltage and frequency control loop of low-voltage islanding operation with inverter-based generation units. This objective is composed of the development of: 1) a new voltage and frequency controller design, 2) a novel multiple inverter voltage and frequency control strategy and 3) a novel grid integration concept for anti-islanding detection, low-voltage ride-through capability and the proposed islanding operation.

The behaviour of low-voltage grids strongly depends on the connected loads and generation units. First, low-voltage grids were analysed and voltage and frequency behaviour was described by the relevant power equations. It was shown, that with an inverter-based generation the active power defines the islanding voltage and the reactive power defines the islanding frequency. The impacts of nonlinear constant power loads were integrated into the overall concept and their effect on voltage stability was derived. Furthermore, the importance and possible impacts of future ancillary services such as low-voltage ride-through capability and anti-islanding detection were described. Representative state-of-the-art inverter control strategies were presented and categorised into grid feeding, grid forming and grid supporting units. Their advantages and disadvantages were investigated with regard to the objectives of this work.

A new controller design for three-phase inverter-based generation in low-voltage grids was proposed. Both voltage and frequency control loops contain a virtual feed-forward admittance and are based on the simplification of the inner current control loop irrespective of the used inverter hardware. Despite existing design methods for voltage frequency control loops, the new design only requires the knowledge of the inverter nominal power rating and the time constant of the inner current control loop, whereas the latter can also be estimated. The transferability and scalability was demonstrated with a control stability analysis. Even if the time constant of the current control loop is miscalculated by a factor of five, the overall voltage control loop was still stable and thus provided a robust control. A two-level three-phase inverter reached nominal grid voltage within a few milliseconds. It was able to maintain nominal values for symmetrical resistive, resistive-inductive and resistive-capacitive loads up to the inverter nominal power and also for nonlinear constant power loads. Even hardly damped open circuit conditions and strongly reactive systems were controlled successfully. The experimental results were obtained using several different laboratory setups to underline the transferability of the design for different
hardware setups: a standard $LCL$ filter without transformer and an intentionally sub-optimally designed $LC$ filter including transformer. Different time constants for the inner current control loop (2 and 4 milliseconds) and the outer voltage control loop (4 and 20 milliseconds) have been implemented. In tests that incorporated a controlled rectifier as a constant power load, the start-up process and several load steps were controlled successfully although there was a relatively high share of harmonics in the system.

A novel multiple inverter control strategy for cooperative voltage and frequency control was developed which incorporates islanding operation for single and multiple inverter setups without the need for communication. It combines the benefits of the existing droop control and the master-slave approach. The multi-inverter operation incorporates a procedure from zero-voltage condition which allows to determine which inverter unit should become the Master unit. The other inverter units become so-called Followers which keep full capability of the Master unit. The procedure from zero-voltage allows to use the full potential of controllable power in the whole island to conjointly reach nominal grid voltage. This allows to start islanding operation for loads that are larger than the largest inverter but still smaller than the sum of all connected inverters. Hence, the chances for successful islanding operation are increased. The cooperative voltage control is based on a dead-band concept. This concept allows to maintain nominal voltage without communication and without circulating steady-state currents among the inverter units. An analogue concept was used for the frequency control. In addition, the dead-band concept contributes to a voltage balancing inside the island in case the line impedances are relatively high. In contrast to existing master-slave approaches, the Master-Follower control strategy is able to compensate an outage of the Master unit. In this case, a Follower takes the lead, detects voltage and frequency deviations and drives them back to nominal values. In experimental tests of up to 6 kW nominal power, two inverters were able to reach nominal voltage and frequency within 200 milliseconds for a linear symmetrical load that was larger than each of the inverters.

Voltage and frequency were controlled at nominal values during several load changes and even in open circuit condition. Furthermore, an outage of the Master unit was compensated by a Follower within a fundamental period and thus islanding operation was maintained.

A new countermeasure against an excess of active power due to non-controllable generation (NCG) was presented. NCG is a possible disturbance in an islanded grid and can result in over-voltage. Existing approaches are limited to a single inverter manufacturer and requires the existence of a battery unit. The new countermeasure can be applied to all generation units in low-voltage grids that provide active reduction due to over-frequency which is a mandatory requirement in existing grid codes. The Master unit increases islanding frequency. Consequently, NCG adapts its active power due to the over-frequency and thus either the increase in power is stopped or active power is even reduced. This allows to operate islanded grids that have NCG which provides almost twice as much active power as needed by the linear resistive loads. The presented functionality has been validated in simulation and in experimental test for a 4 kW system.

A novel concept was developed that provides a possible solution for the grid integration of intentional islanding operation in combination with low-voltage ride-through capability (LVRT) and anti-islanding detection (AID). The novel concept incorporates a time decoupling. Conflicting aims of the three domains were dissolved and their compatibility was scrutinised with the help of a case study. In this case study, possible outcomes of both grid faults and unintentional islanding were derived. Asymmetrical faults were also included. It was initially shown that the effectiveness of AID is not undermined if LVRT is implemented simultaneously. LVRT capability even improved the effectiveness of AID because islands were detected very quickly. Subsequently
to the fault behaviour, the novel islanding control strategies for single and multiple inverter operation was initiated including the procedure from zero-voltage condition. In laboratory tests, the novel concept was demonstrated for a 8 kW inverter setup.

A discussion of open issues and future challenges with regard to islanding operation concluded this work. Additional research is needed for asymmetrical and nonlinear load conditions. Besides, motor loads and rotating generators were not included in this work and require special attention as they strongly influence transient and steady-state behaviour of islanded grids. This could also influence multiple inverter operation and the countermeasure against an excess of active power. Future research is required in case the allocation of Master and Follower unit fails and what effects occur if there are multiple Masters in a single island. Finally, the most challenging task for the implementation of intentional islanding operation in low-voltage grids might be the development of a safe and reliable grid integration concept. There is an extensive need for research that provides solutions for the transition from islanding back to grid parallel operation, controlled shut-down procedures due to maintenance works and suitable protection schemes to ensure safe operation even in response to abnormal grid conditions.
Appendix A

Single-Phase Transformation and Transformation Matrices

Voltage Calculation for Single-Phase Equivalent Circuit

In the single-phase equivalent circuit, the line-to-neutral voltages $V_a$, $V_b$ and $V_c$ are used. In a symmetrical system they can be calculated from the line-to-line voltages $V_{ab}$, $V_{bc}$ and $V_{ca}$ with the following equation:

$$V_a = \frac{1}{3} \cdot (V_{ab} - V_{ca}) \ , \ V_b = \frac{1}{3} \cdot (V_{bc} - V_{ab}) \ , \ V_c = \frac{1}{3} \cdot (V_{ca} - V_{bc}) \quad (A.1)$$

Clarke Transformation and Park Transformation

For the transformation from natural $abc$ frame to $\alpha\beta$ frame, the Clarke transformation is used:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (A.2)$$

For the transformation from $\alpha\beta$ frame to $dq$ frame, the Park transformation is used:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos \varphi & \sin \varphi \\ -\sin \varphi & \cos \varphi \end{bmatrix} \cdot \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \quad (A.3)$$

For the transformation from $dq$ frame to $\alpha\beta$ frame, the inverse Park transformation is used:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} \cos \varphi & -\sin \varphi \\ \sin \varphi & \cos \varphi \end{bmatrix} \cdot \begin{bmatrix} V_d \\ V_q \end{bmatrix} \quad (A.4)$$

For the transformation from $\alpha\beta$ frame to natural $abc$ frame, the Clarke transformation is used:

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & \frac{1}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{1}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \quad (A.5)$$
Appendix B

Transfer Functions

Transfer Function of the Voltage Control Loop

The block diagram of the voltage control loop can be rearranged and finally simplified to:

\[
F_{W,V}(s) = \frac{1}{\frac{1}{R_{ff}} - \frac{1}{r_{CC}} + \frac{1}{F_{PWM}} + \frac{1}{r_{Li} \cdot F_{CF} \cdot F_{PWM}} + \frac{1}{r_{Lg} \cdot r_{Li} \cdot F_{PWM}}} \cdot \left(1 + \frac{F_{Lg} + F_{Li} + \frac{1}{r_{CF}}}{r_{Lg} \cdot r_{Li} \cdot F_{PWM}}\right)
\]

\[
= \frac{1}{\frac{1}{R_{ff}} - \frac{1}{r_{CC}} + \frac{1}{F_{PWM}} + \frac{1}{r_{Li} \cdot F_{CF} \cdot F_{PWM}} + \frac{1}{r_{Lg} \cdot r_{Li} \cdot F_{PWM}}} - \frac{F_{Lg} + F_{Li} + \frac{1}{r_{CF}}}{r_{Lg} \cdot r_{Li} \cdot F_{PWM}}
\]

\[
= \frac{R_{L} \cdot R_{ff} \cdot F_{CC} \cdot F_{PWM} \cdot F_{Lg} \cdot F_{Li} \cdot F_{CF}}{A - B - C + D + E + F + R_{ff} + G}
\]

with:

\[
A = R_{ff} F_{CC} F_{PWM} F_{Lg} F_{Li} F_{CF}
\]

\[
B = R_{L} R_{ff} F_{PWM} F_{Lg} F_{Li} F_{CF}
\]

\[
C = R_{L} R_{ff} F_{Lg} F_{Li} F_{CF}
\]

\[
D = R_{ff} F_{Li} F_{CF}
\]

\[
E = R_{ff} F_{CF} F_{Lg}
\]

\[
F = R_{L} R_{ff} F_{Lg}
\]

\[
G = R_{L} F_{CC} F_{PWM} F_{Lg} F_{Li} F_{CF}
\]
Transfer Function of Filter Components

Figure B.1 shows voltages and currents for an LCL and an L filter. The grid side current $I_g$ in an L filter including resistive components $R$ can be calculated with:

$$I_g = \frac{V_t}{R + j\omega L} \quad (B.9)$$

The current in an LCL filter can be calculated by splitting the filter into two transfer functions. The calculation of the grid side current $I_g$ is:

$$I_g = \frac{V_C}{R_g + j\omega L_g} \quad (B.10)$$

Using the parallel impedance $X||$:

$$X|| = X_C \cdot X_{RL} = \frac{j\omega L_g + R_g}{1 + j\omega R_g C_F - \omega^2 L_g C_F} \quad (B.11)$$

The capacitor voltage $V_C$ can be calculated with the transfer function:

$$\frac{V_C}{V_t} = \frac{X||}{X|| + R_i + j\omega L_i} = \frac{R_g + j\omega L_g}{j\omega L_g + R_g + j\omega L_i + R_i + (R_i + j\omega L_i) \cdot (j\omega R_g C_F - \omega^2 L_g C_F)} \quad (B.12)$$

This allows to calculate the grid side current $I_g$ as a function of the terminal voltage $V_t$:

$$I_g = \frac{V_t}{R + j\omega L + j\omega R_g R_i C_F - \omega^2 C_F \cdot (L_g R_i + L_i R_g) - j\omega^3 L_i L_g C_F} \quad (B.13)$$

Figure B.2 shows the transfer functions $I_g/V_t(s)$ of an L and an LCL filter (undamped and damped) in a Bode plot. It can be seen that the transfer functions are almost identical below $f = 1$ kHz. Thus, for control time constants of $\tau_i > 1$ ms, an LCL filter can be approximated with an L filter.
Figure B.2: Bode diagram of an $L$ and an $LCL$ filter. Only for $f \geq 1$ kH, the transfer functions differ significantly in both magnitude (a) and phase (b).
Appendix C

Bode Diagrams for Scalability

Figure C.1: Bode diagram of several inverter power ratings and PWM frequencies (1).

(A) $P = 1 \text{ kW}, f_{PWM} = 5 \text{ kHz}$.

(B) $P = 1 \text{ kW}, f_{PWM} = 10 \text{ kHz}$.

(C) $P = 1 \text{ kW}, f_{PWM} = 20 \text{ kHz}$.

(D) $P = 10 \text{ kW}, f_{PWM} = 5 \text{ kHz}$.
Figure C.2: Bode diagram of several inverter power ratings and PWM frequencies (2).
Appendix D

Experimental Results for an LC Transformer Setup

Figure D.1: Single-phase equivalent Circuit for the inverter setup incorporating an LC filter and a transformer.

Figure D.1 shows the experimental setup for an inverter that is equipped with an LC filter and a transformer. The actual filter design was intentionally sub-optimal to illustrate the effects on current, voltage and frequency control. Table D.1 contains the controller variables. In this case, a slower current and voltage control loop was designed (τ_i = 4 ms, τ_V = 20 ms). Figure D.2 and Figure D.3 show the results for the voltage and the current control loop respectively. The model (grey area) provides a good prediction of the behaviour of the voltage control loop. The weaknesses of the LC filter and transformer design mainly affect the current control loop. Thus, the voltage control loop faces relatively high transients especially for small damping in the system.

Table D.1: Parameters of the experimental tests for single-inverter operation with an LC filter and transformer setup.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>P_n</td>
<td>Nominal power of the inverter</td>
<td>8 kVA</td>
</tr>
<tr>
<td>L_iL_T</td>
<td>Filter inductances</td>
<td>2.4 / 9.6 mH</td>
</tr>
<tr>
<td>C_F</td>
<td>Filter capacitance</td>
<td>4.7 µF</td>
</tr>
<tr>
<td>r_T</td>
<td>Transformer ratio</td>
<td>230/100 V</td>
</tr>
<tr>
<td>τ_i</td>
<td>Time constant of the current controller</td>
<td>4 ms</td>
</tr>
<tr>
<td>τ_V</td>
<td>Time constant of the voltage controller</td>
<td>20 ms</td>
</tr>
<tr>
<td>τ_f</td>
<td>Time constant of the frequency controller</td>
<td>22 ms</td>
</tr>
<tr>
<td>T_s</td>
<td>Sampling time of the control loops</td>
<td>200 µs</td>
</tr>
<tr>
<td>f_PWM</td>
<td>Switching frequency of the PWM</td>
<td>10 kHz</td>
</tr>
</tbody>
</table>
Figure D.2: Step response of the voltage control loop for various resistive (a), resistive-inductive (b) and resistive-capacitive (c) load conditions. Comparison with the mathematical model (grey area). $\tau_v = 20\,\text{ms}$. 

\[\tau_i = 4\,\text{ms}, \quad \tau_V = 20\,\text{ms}, \quad Q_{L,C} = 0\]

\[\tau_i = 4\,\text{ms}, \quad \tau_V = 20\,\text{ms}, \quad Q_L = 0.50\,P_n\]

\[\tau_i = 4\,\text{ms}, \quad \tau_V = 20\,\text{ms}, \quad Q_C = 0.50\,P_n\]
Figure D.3: Disturbance reaction of the frequency control loop for various resistive (a), resistive-inductive (b) and resistive-capacitive (c) load conditions. \( \tau_i \approx 20 \text{ ms}. \)
Appendix E

Experimental Setups

Figure E.1: Experimental setup incorporating an LCL filter without transformer, using a dSpace DS1007 control system.
Figure E.2: Experimental setup incorporating an LC filter and a transformer, using a dSpace DS1005 control system and a three-phase Semicon IGBT inverter unit with additional driver devices.
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